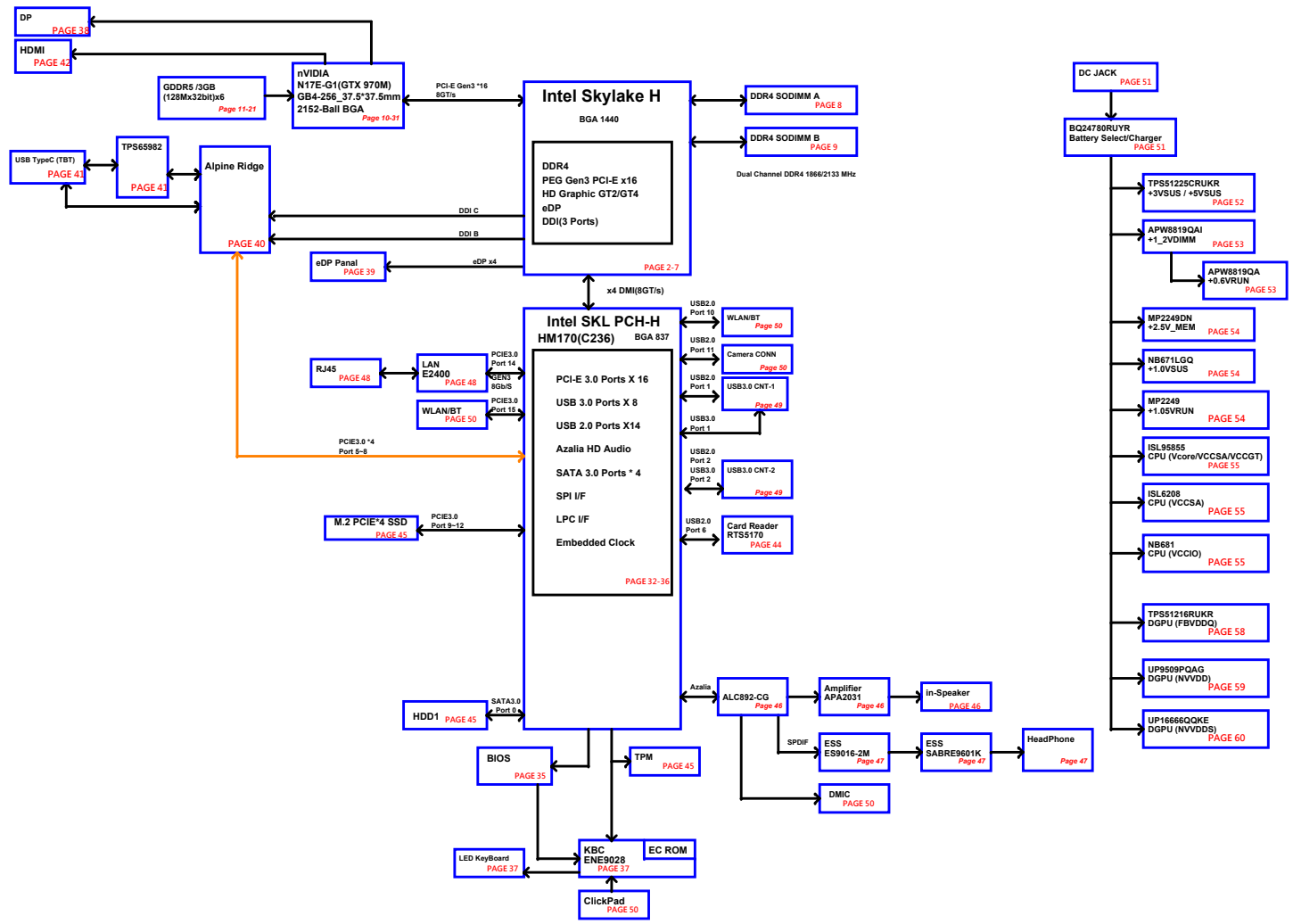
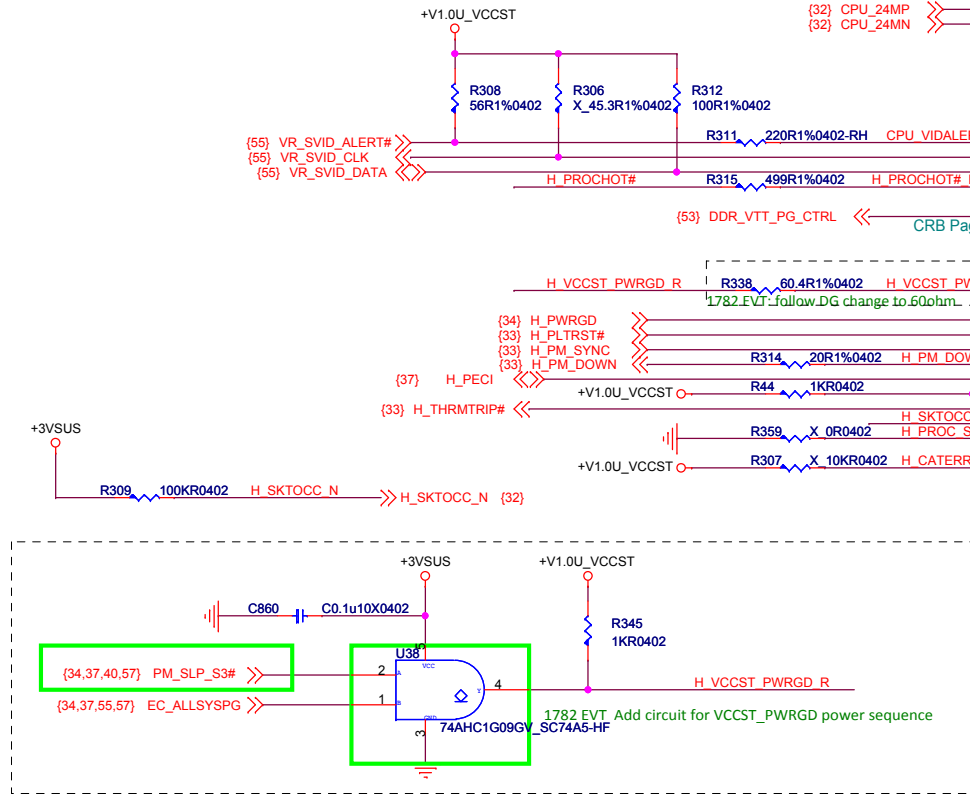
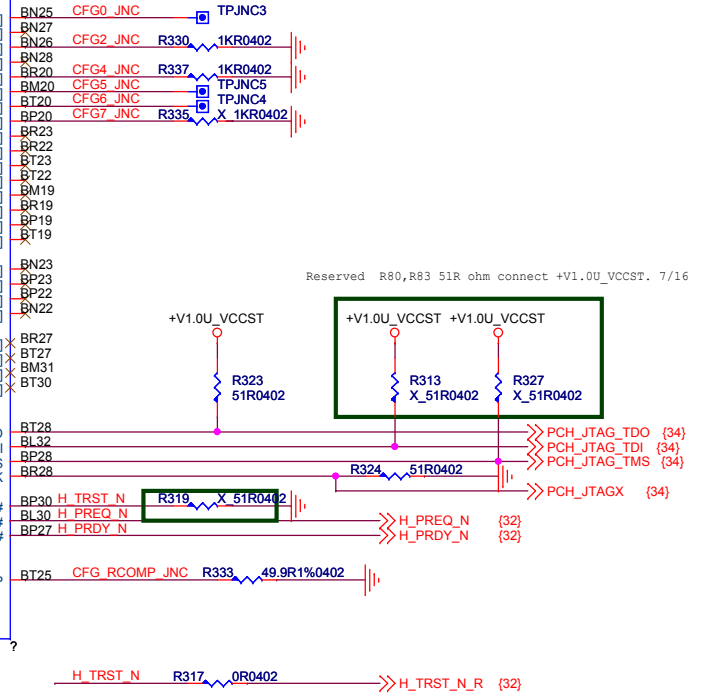
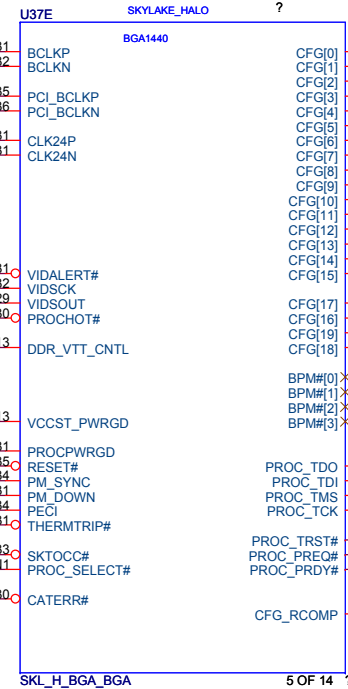
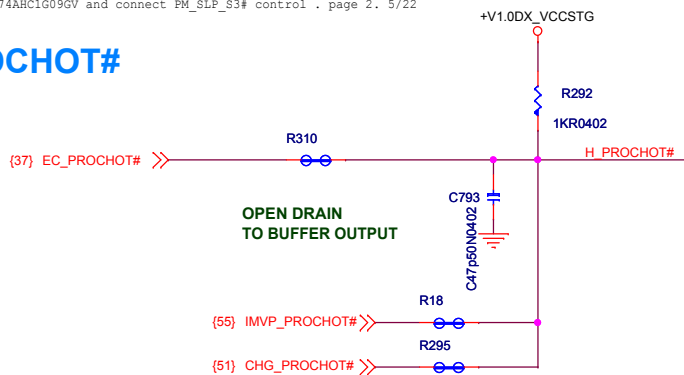


Page 01: Block Diagram
Page 02: Skylake(HOST)
Page 03: Skylake(DDR4)
Page 04: Skylake(DMI/DISPLAY)
Page 05: Skylake(Power)
Page 06: Skylake(Power)
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Page 68: A|LED
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PROCHOT#



MSR Privacy Bit Feature	
CFG3	1 = Debug capability is determined by IA32_Debug_Interface_MSR (0xC80) bit[0] setting 0 = IA32_Debug_Interface_MSR (0xC80) bit[0] default setting overridden

eDP Enable	
CFG4	1 = Disabled 0 = Enabled

PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

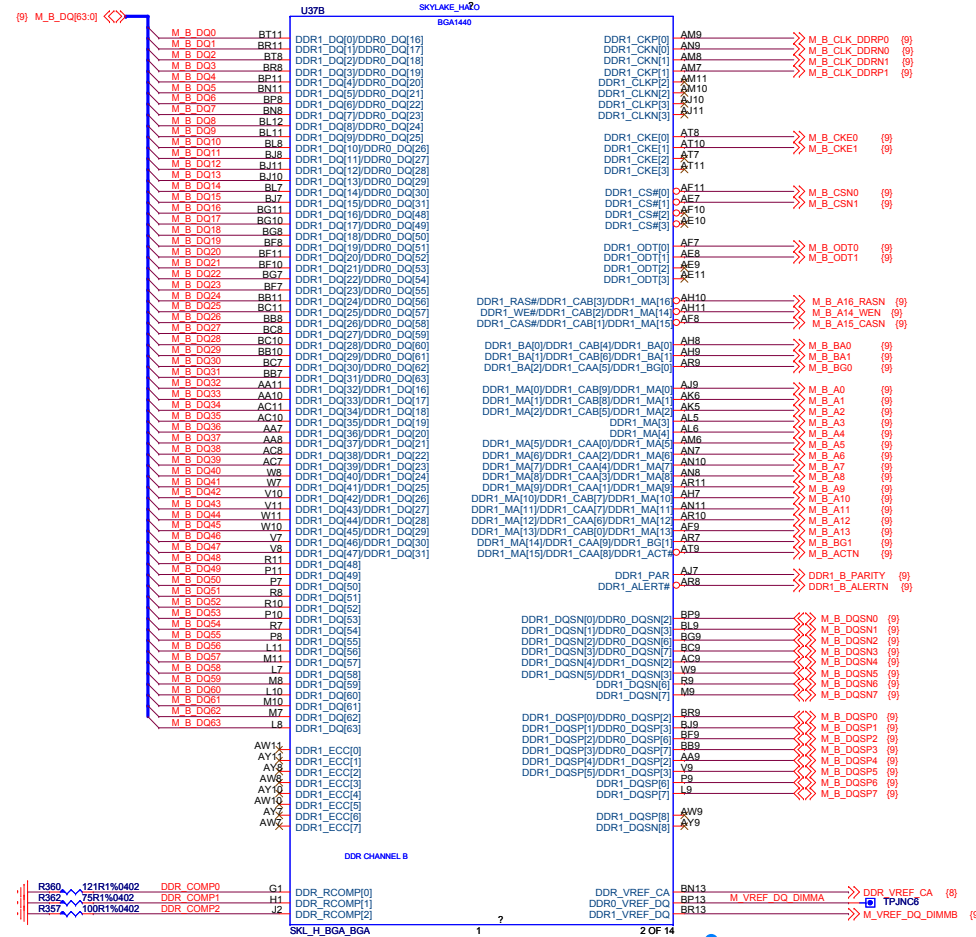
PCI Express * Static X16 Lane Numbering Reversal	
CFG2	CFG[2]: PCI Express* Static x16 Lane Numbering Reversal. 1 = Normal operation 0 = Lane numbers reversed.

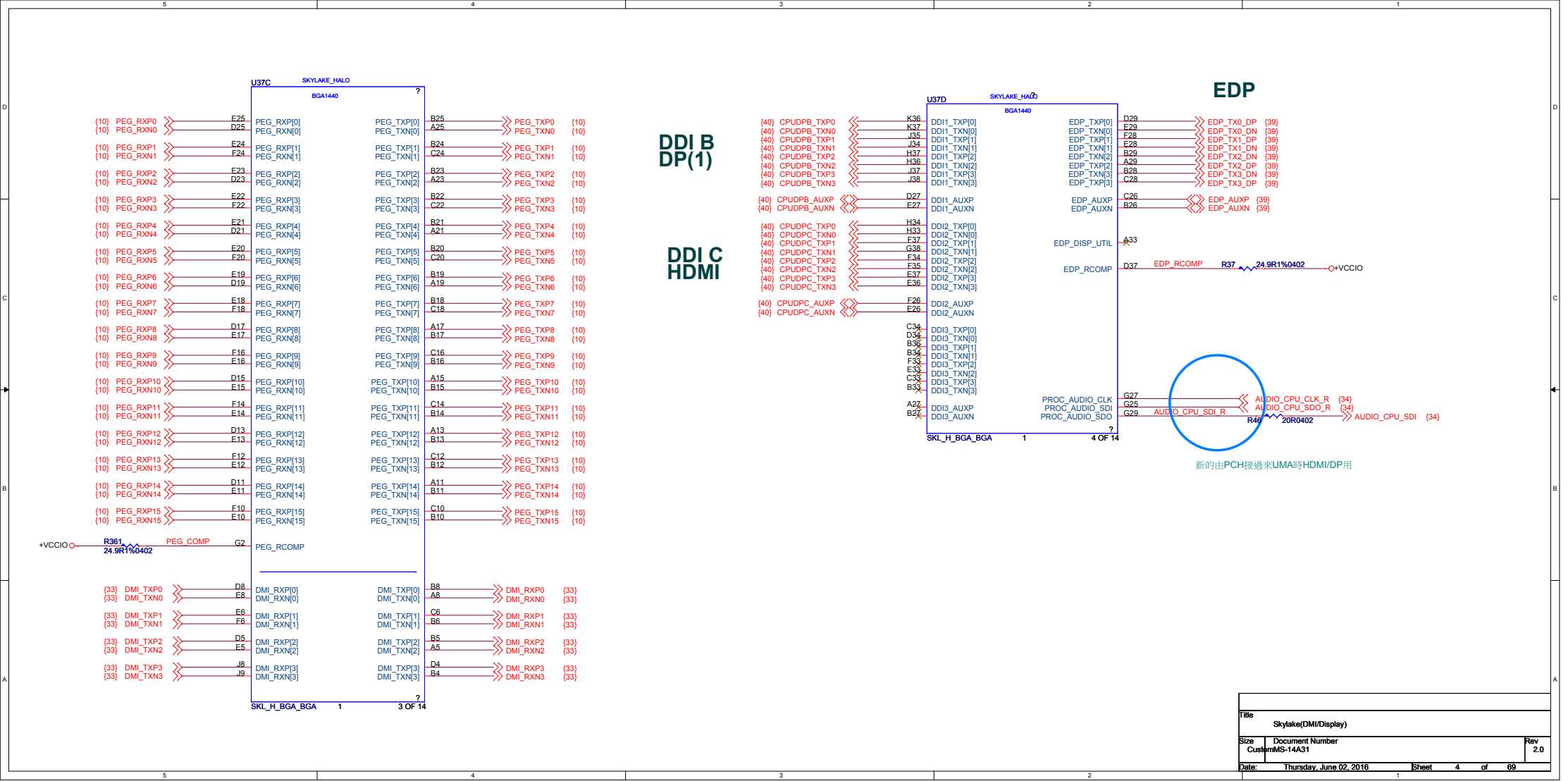
PCI Express* Bifurcation	
CFG[6:5]	00 = 1 x8, 2 x4 PCI Express* 01 = reserved 10 = 2 x8 PCI Express* 11 = 1 x16 PCI Express*

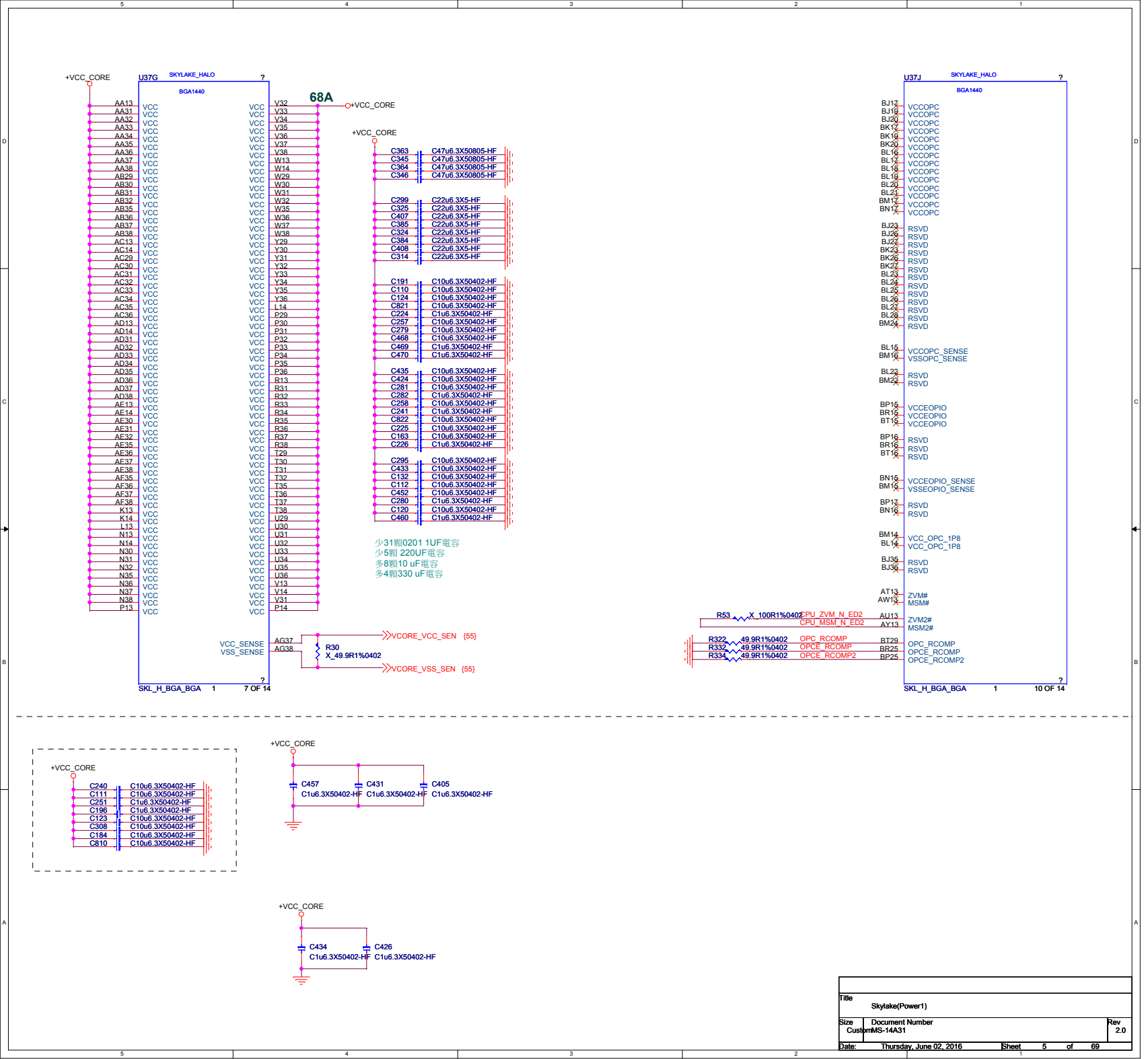
Intel 54492 Page 37,121

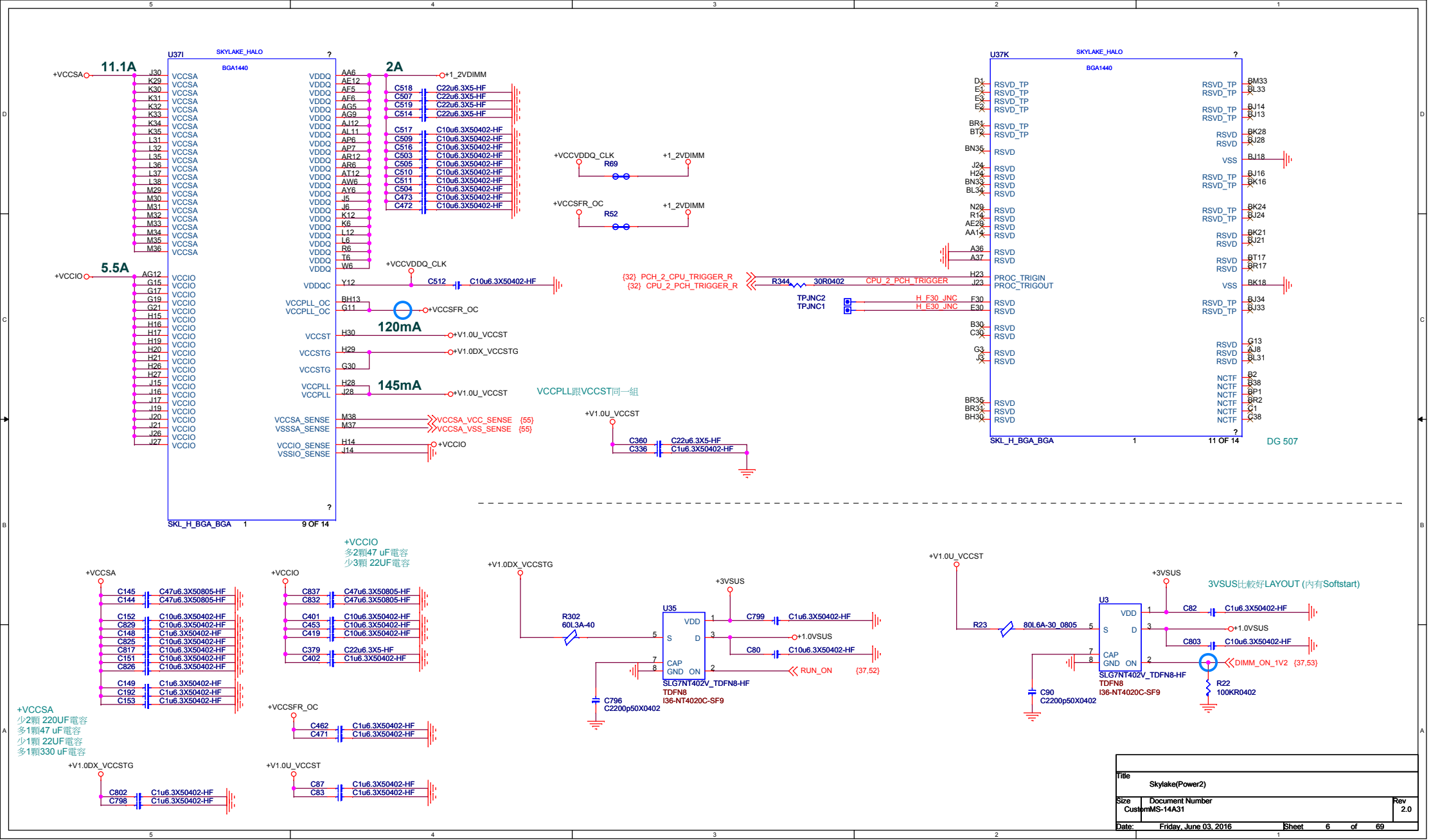
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Skylake(HOST)		
Size	Document Number	Rev
Custom	MS-14A31	2.0
Date:	Thursday, June 02, 2016	Sheet 2 of 69

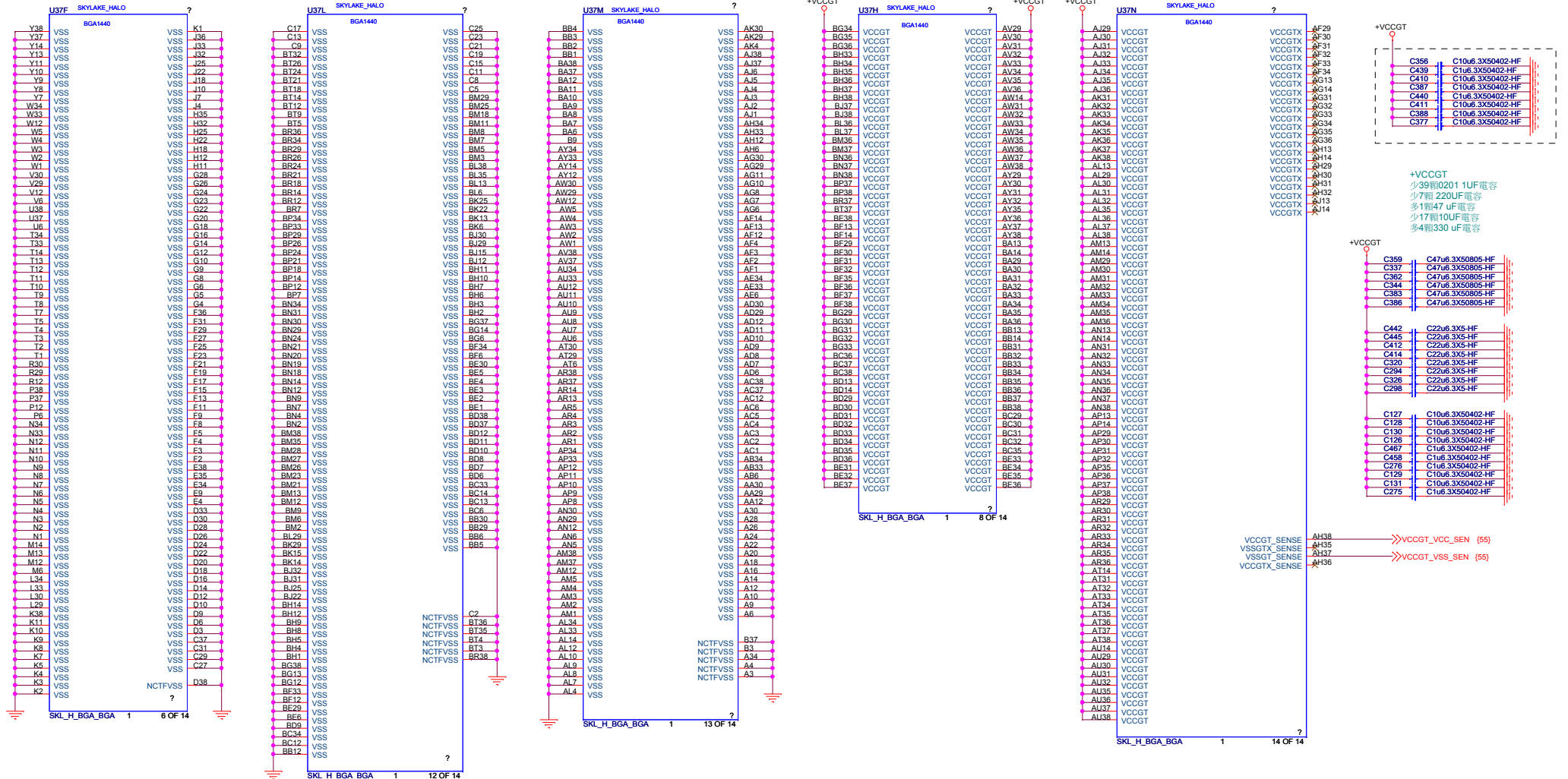
DDR Channel B



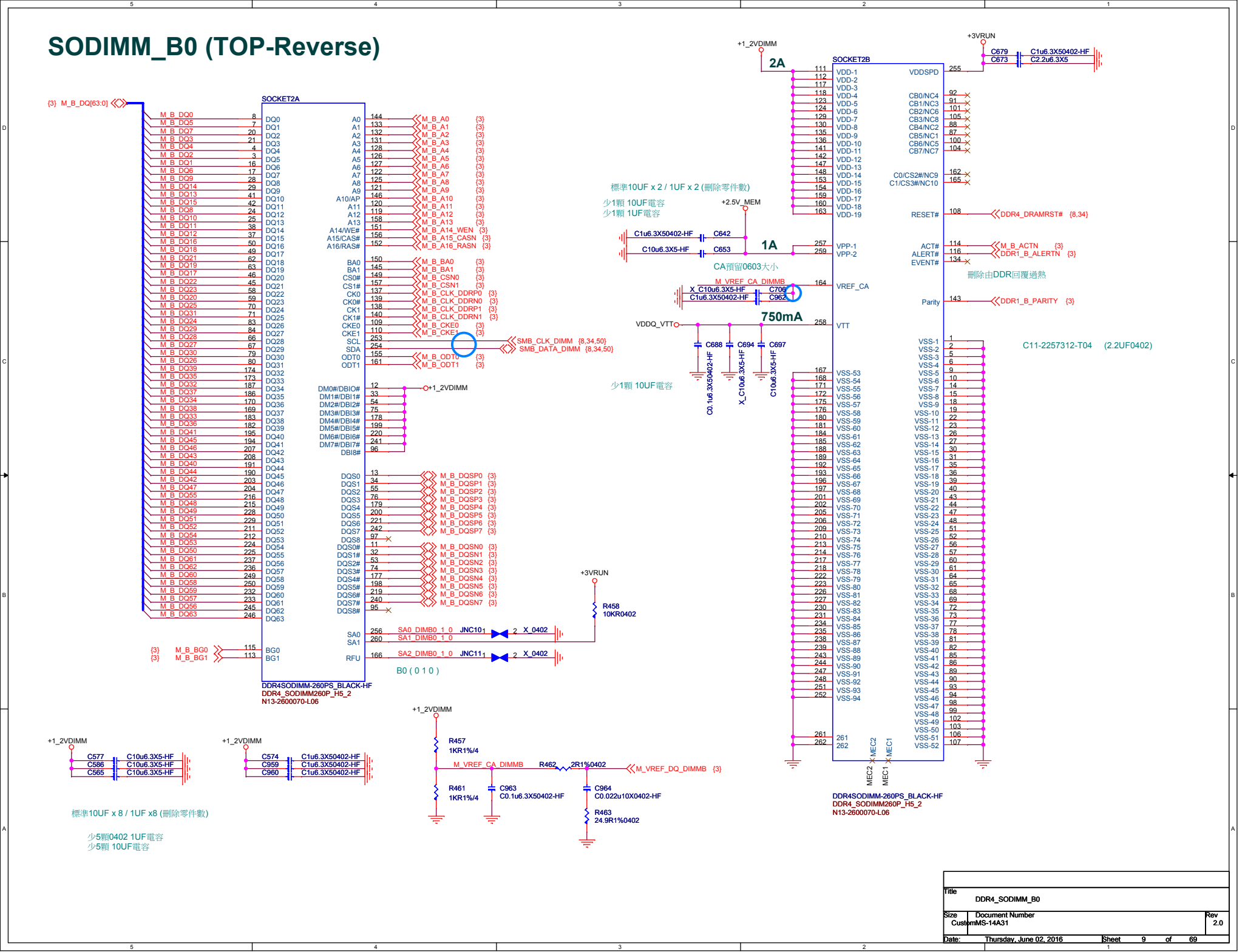




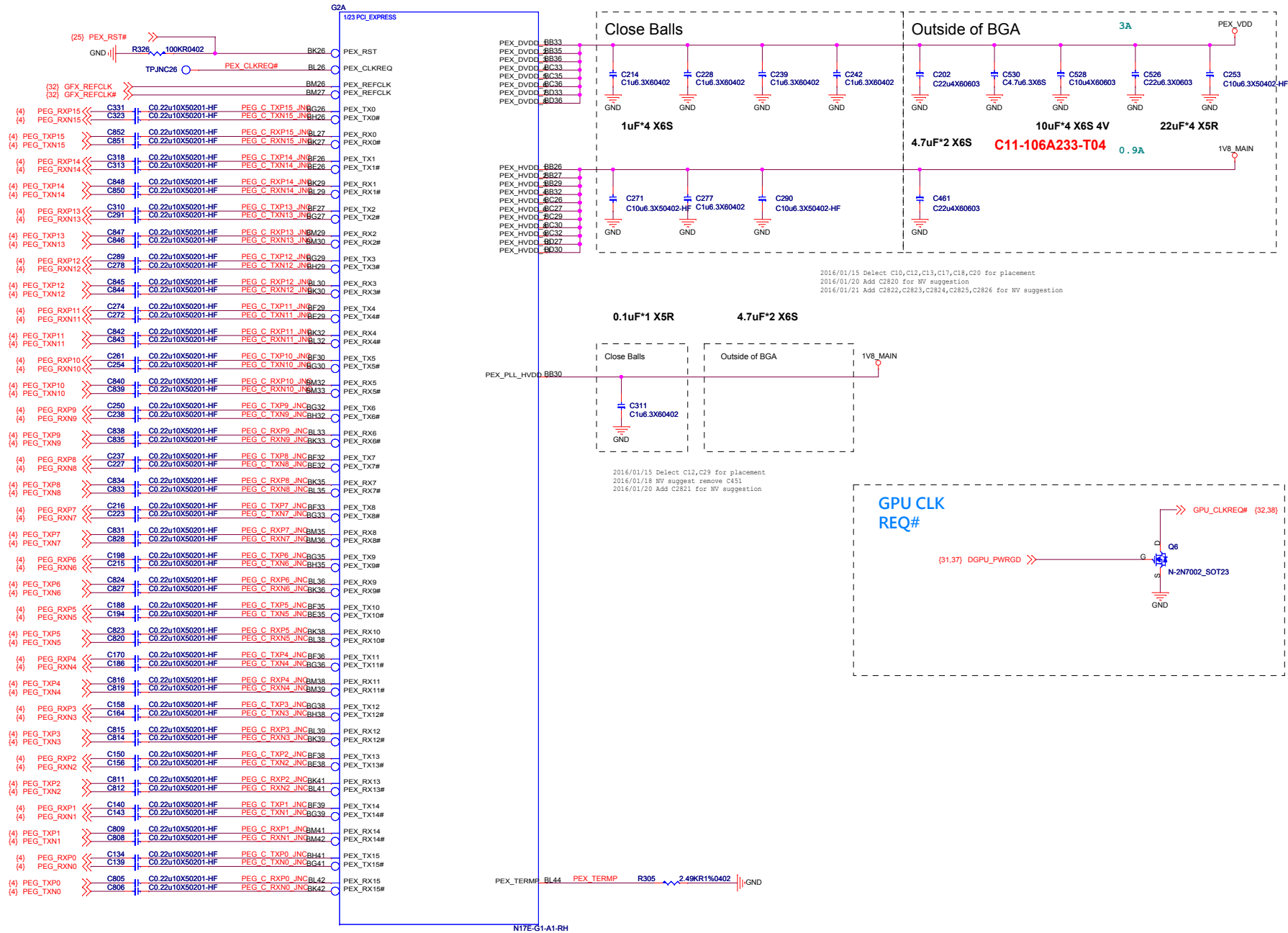




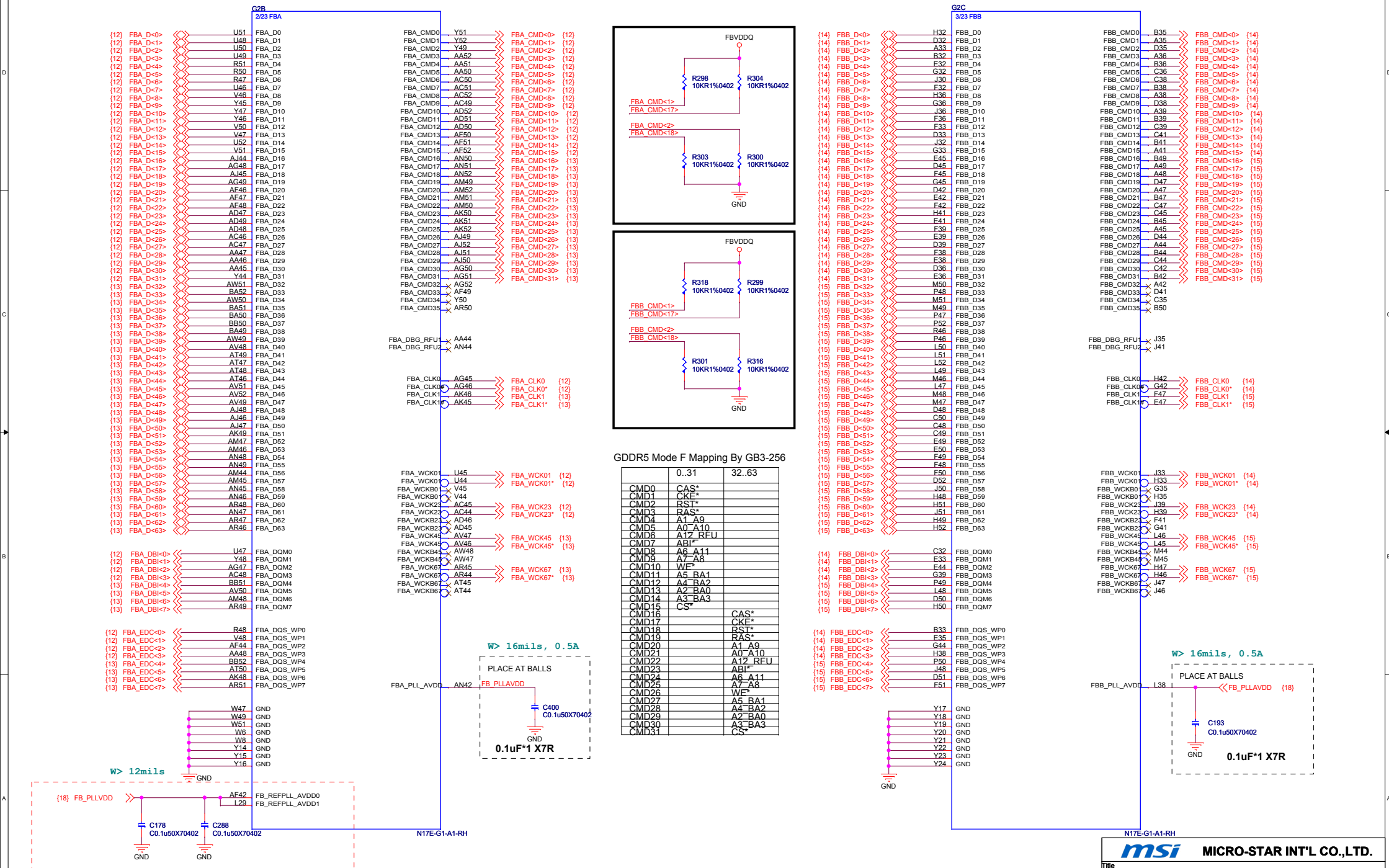
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DDR4_SODIMM_A0				
Size	Document Number			Rev
Custom	MS-14A31			2.0
Date:	Thursday, June 02, 2016	Sheet	8 of 69	

[illegible][illegible]

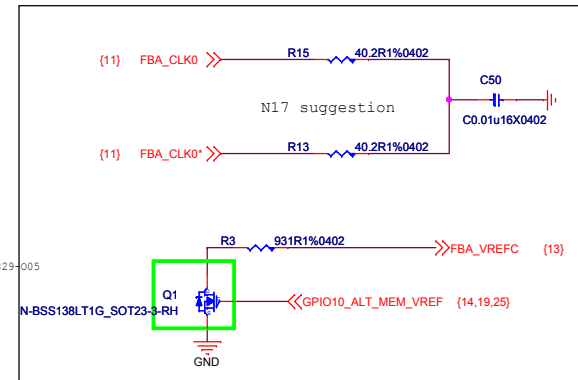
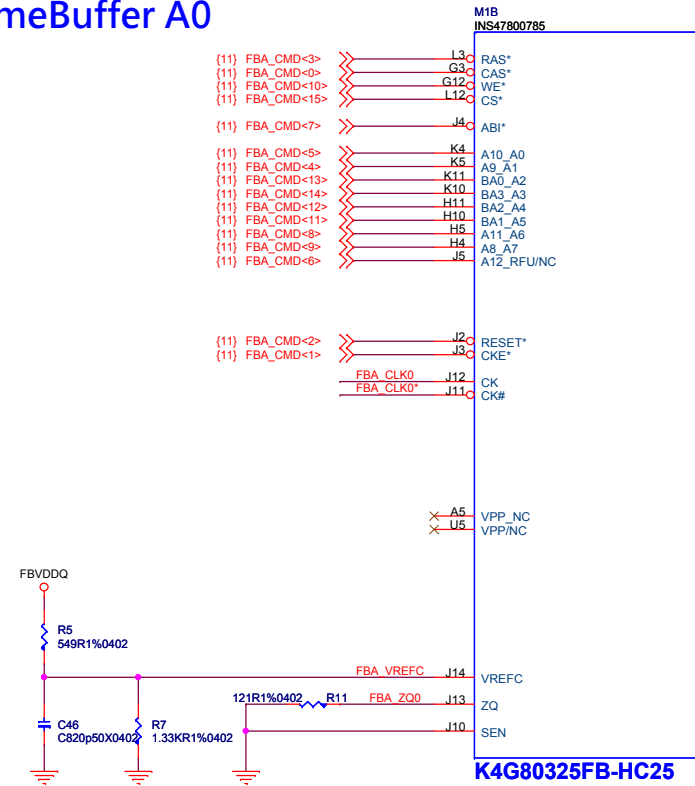
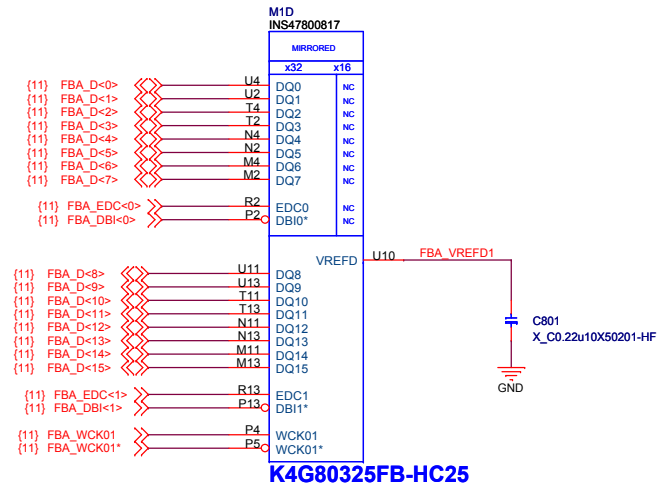
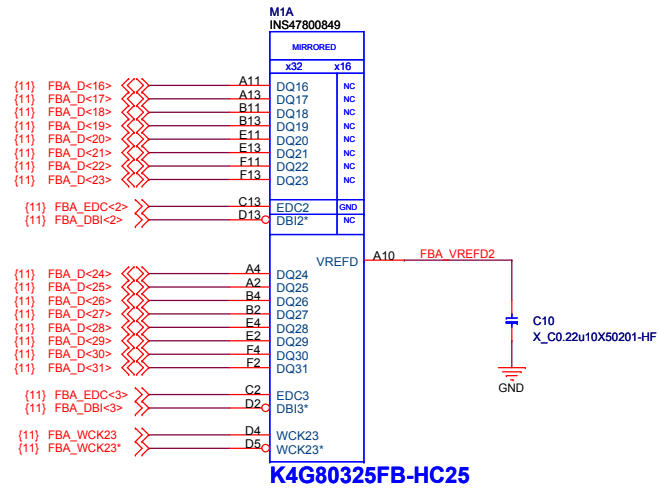
GPU PCI EXPRESS



GPU Frame Buffer Partition A/B



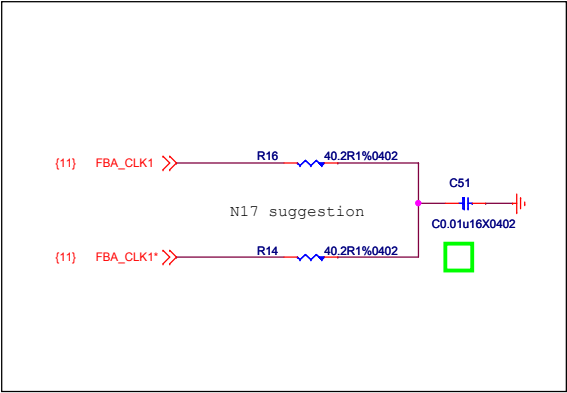
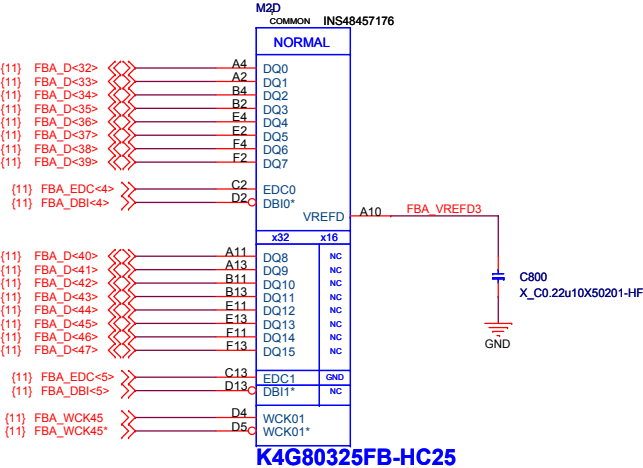
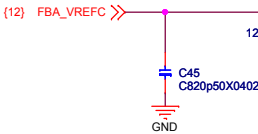
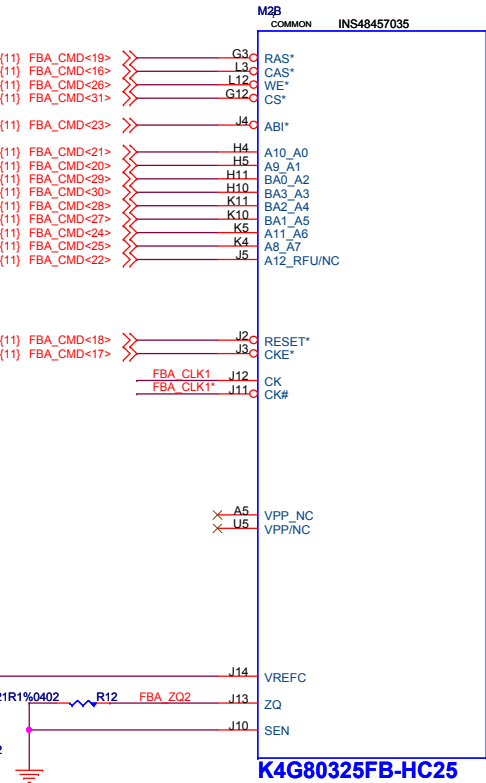
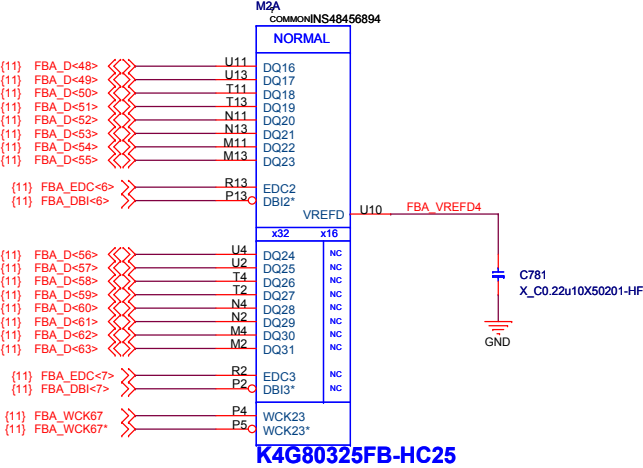
DGPU_GDDR5 FrameBuffer A0



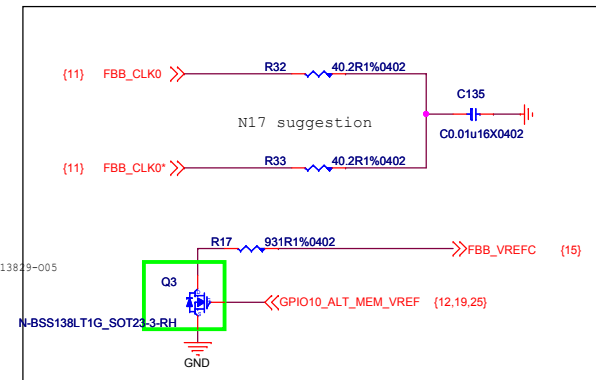
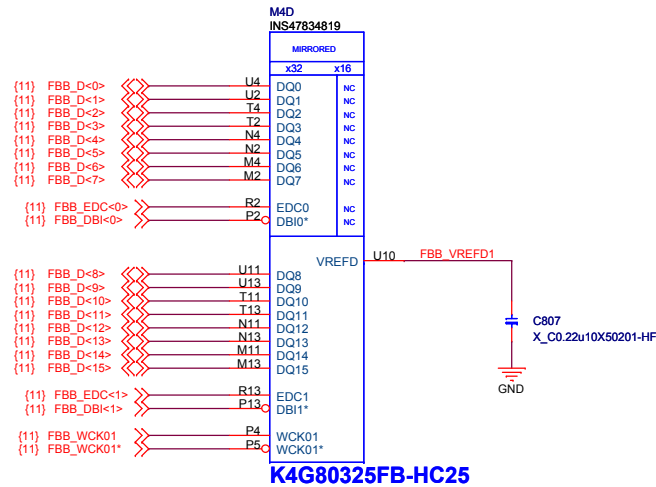
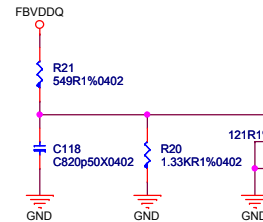
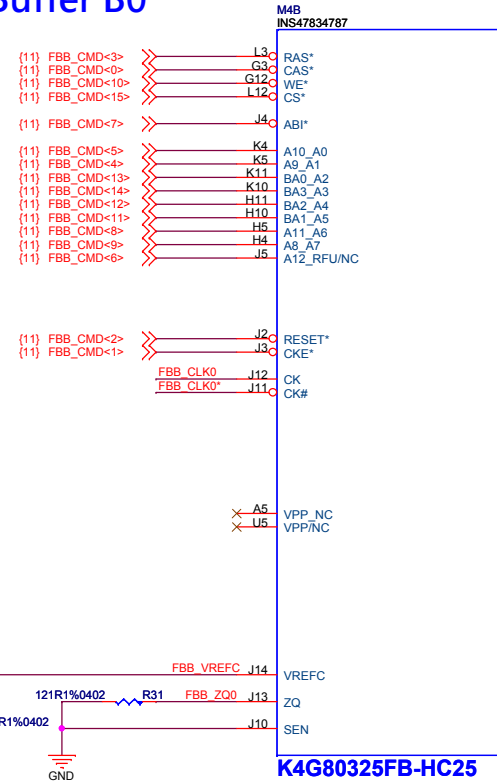
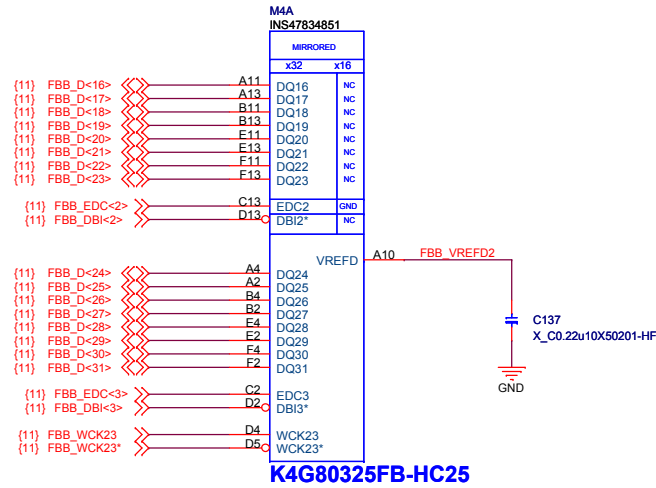
2016/05/12 Q1 change to D03-0013823-005

未定
Hynix PN : M12-5GC4H65-H23 3G(128Mx32bit)
Samsung PN : M12-4132525-S02 3G(128Mx32bit)

DGPU_GDDR5 FrameBuffer A1

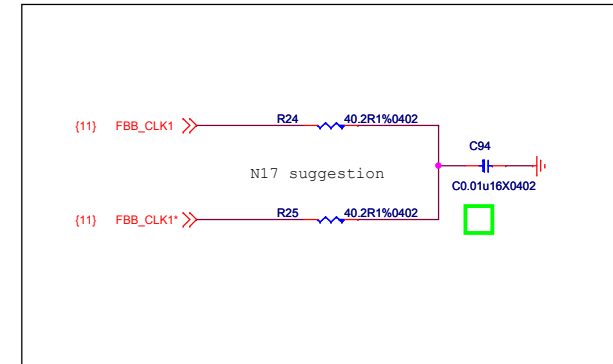
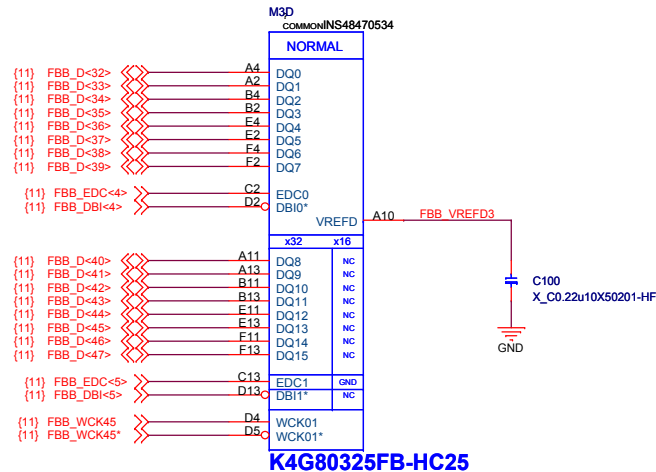
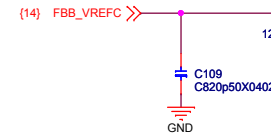
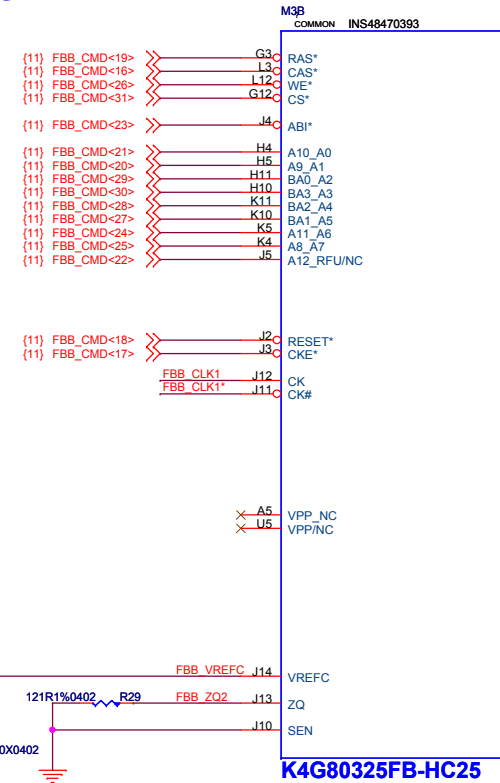
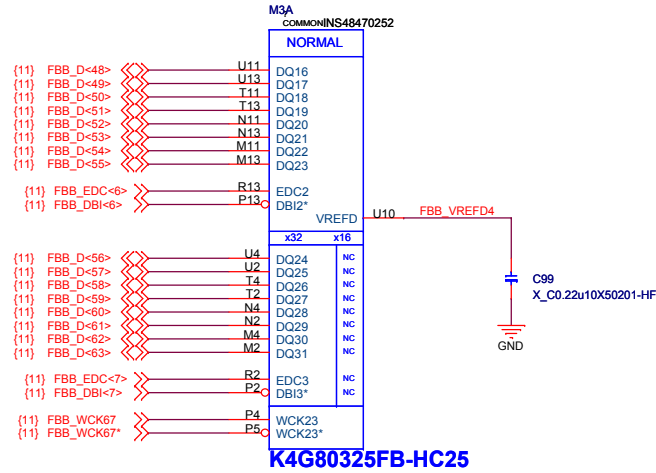


DGPU_GDDR5 FrameBuffer B0

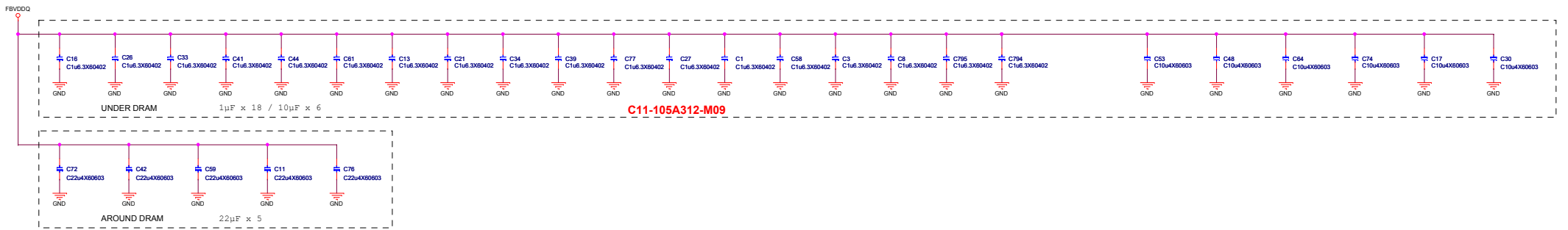
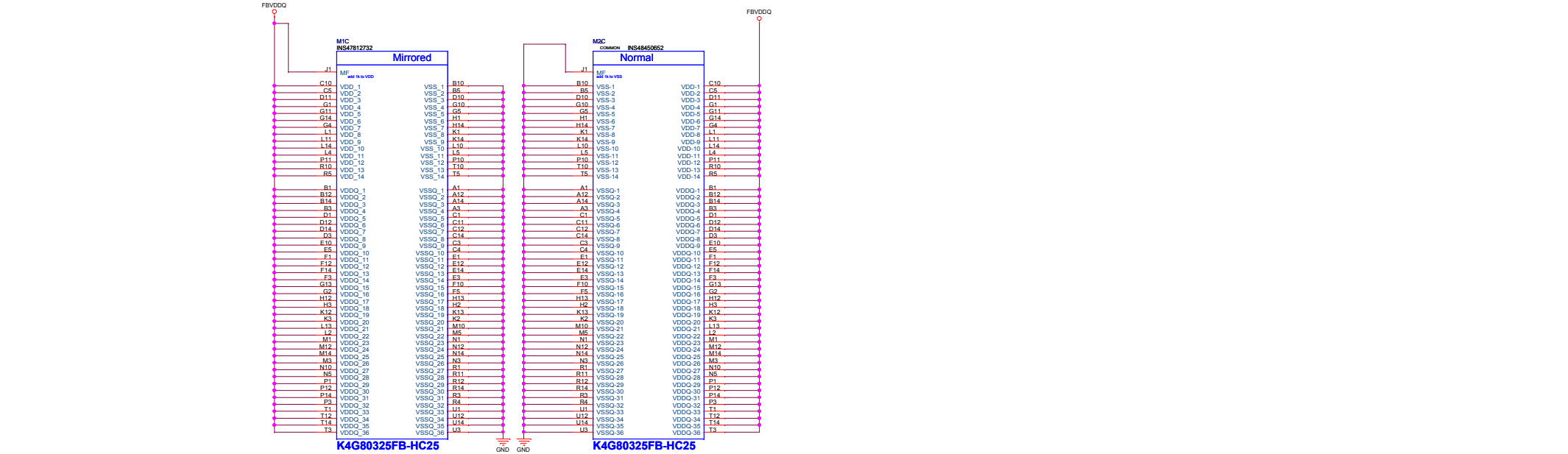
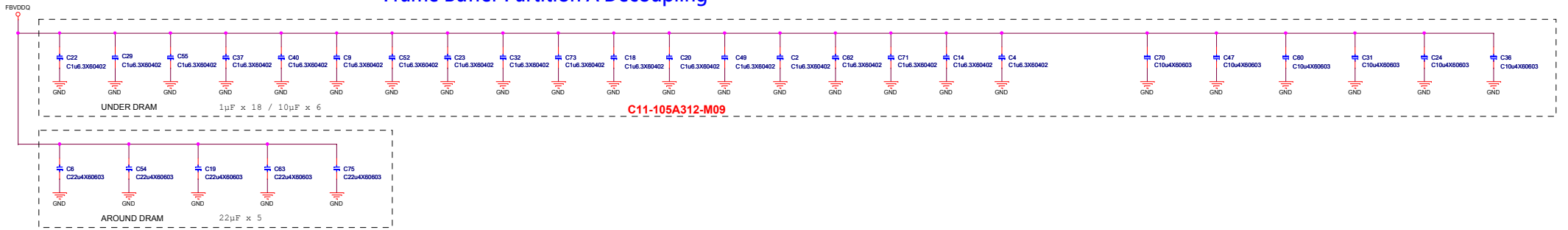


2016/05/12 Q3 change to D03-0013829-005

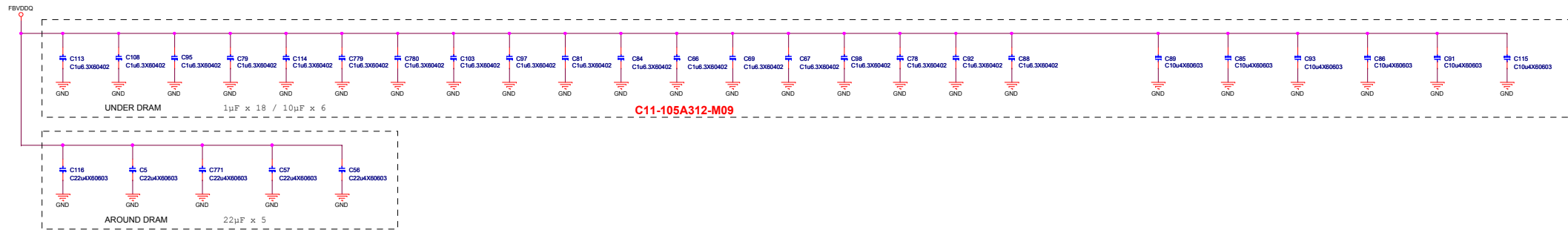
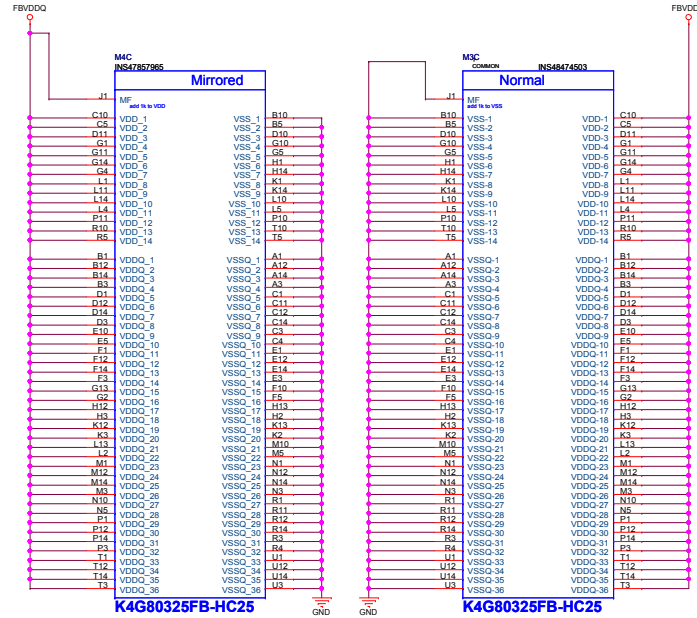
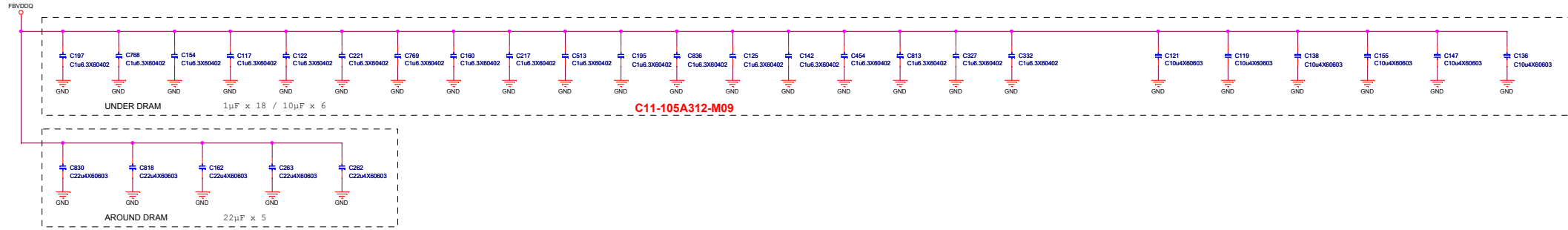
DGPU_GDDR5 FrameBuffer B1



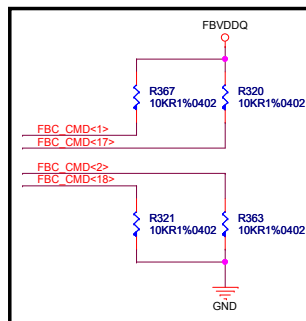
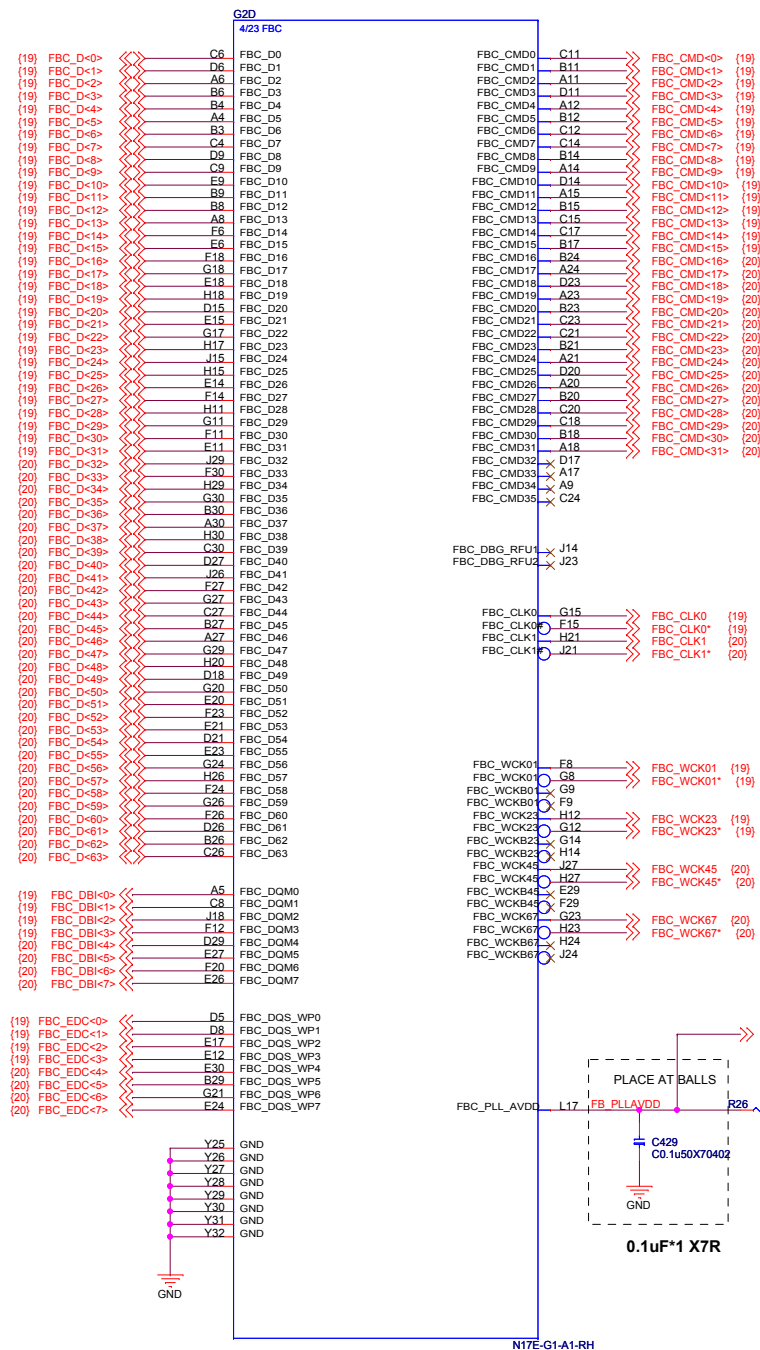
Frame Buffer Partition A Decoupling



Frame Buffer Partition B Decoupling

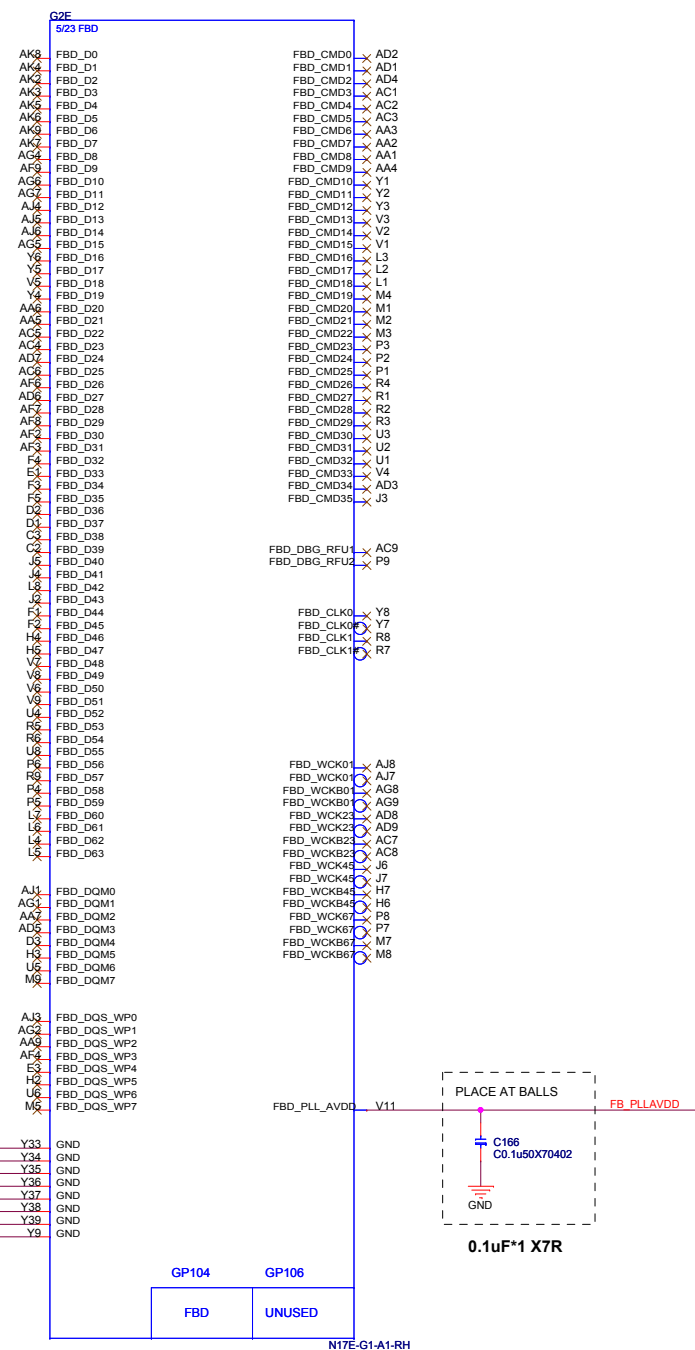


GPU Frame Buffer Partition C/D

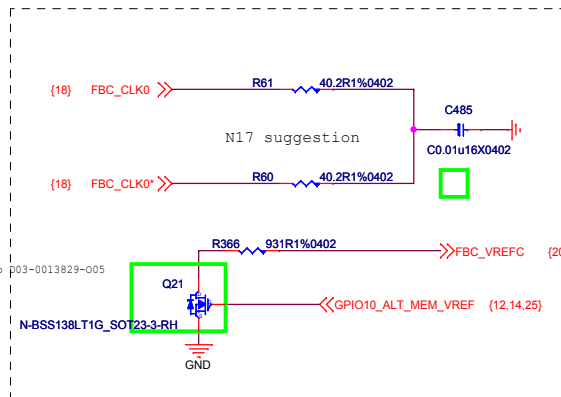
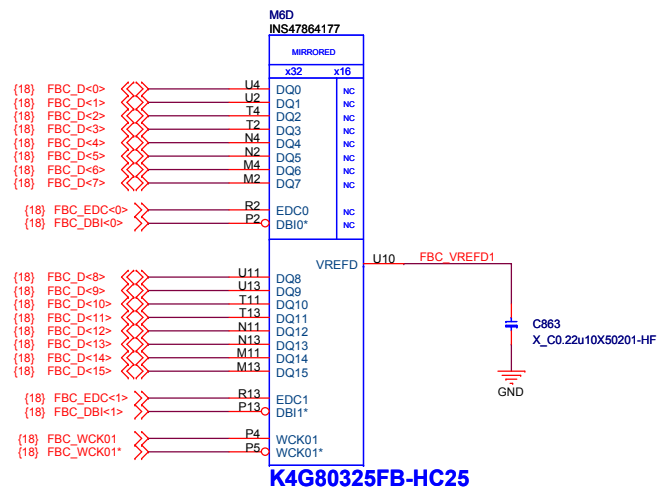
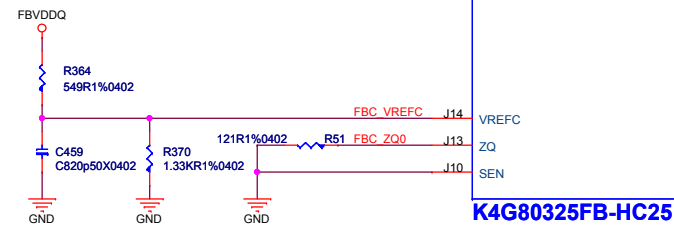
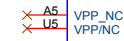
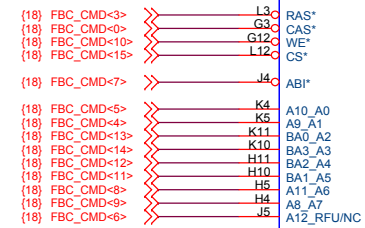
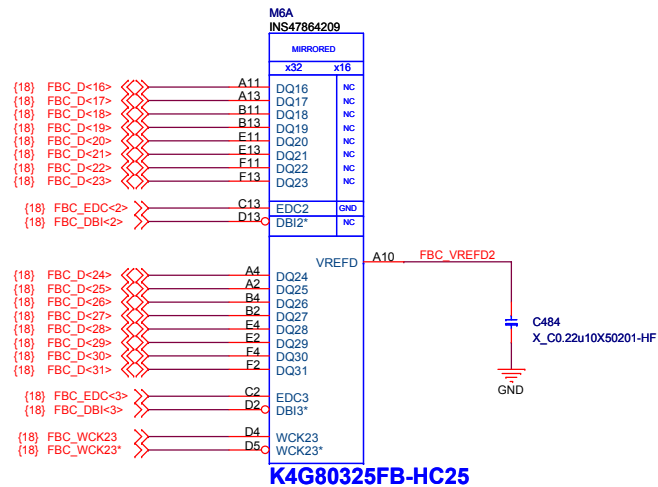


GDDR5 Mode F Mapping By GB3-256

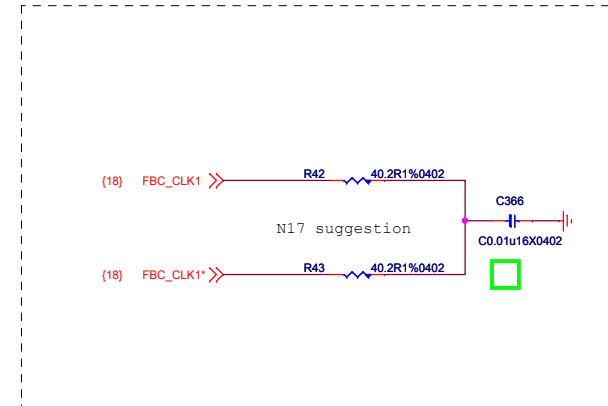
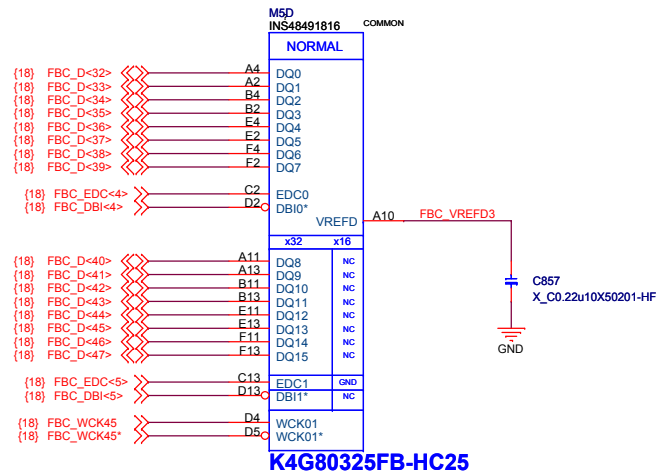
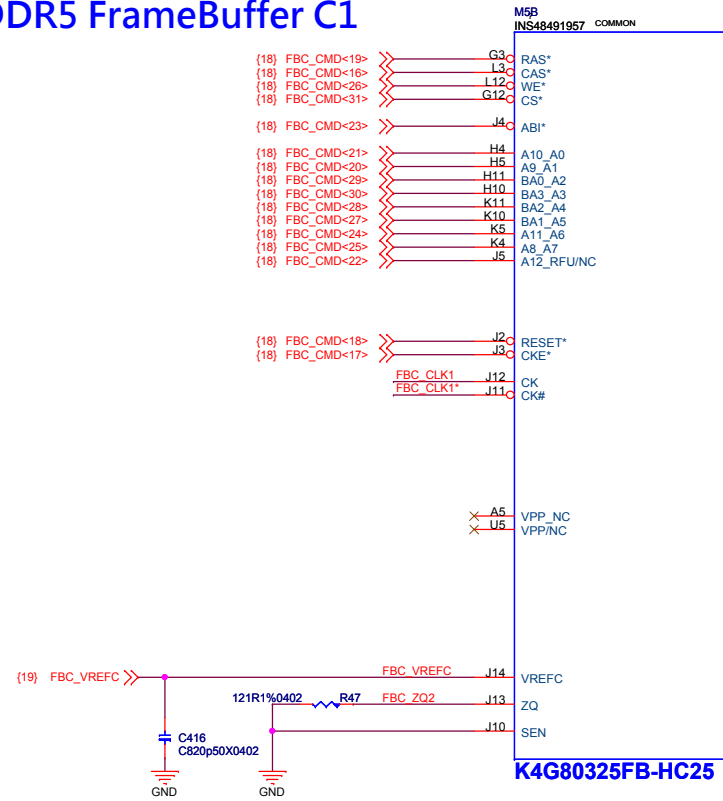
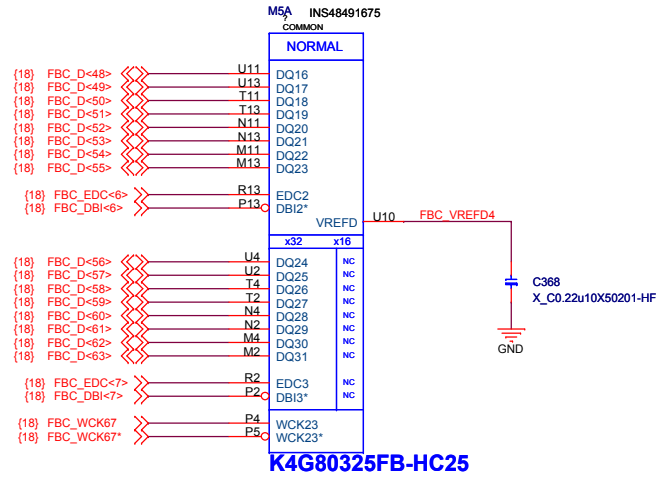
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CMD0	CAS*	
CMD1	CKE*	
CMD2	RST*	
CMD3	RA*	
CMD4	A1 A9	
CMD5	A0 A10	
CMD6	A17 RFU	
CMD7	AB1*	
CMD8	A6 A11	
CMD9	A7 A8	
CMD10	WE*	
CMD11	A5 BA1	
CMD12	A4 BA2	
CMD13	A2 BA0	
CMD14	A3 BA3	
CMD15	CS*	
CMD16		CAS*
CMD17		CKE*
CMD18		RST*
CMD19		RA*
CMD20	A1 A9	
CMD21	A0 A10	
CMD22	A17 RFU	
CMD23	AB1*	
CMD24	A6 A11	
CMD25	A7 A8	
CMD26	WE*	
CMD27	A5 BA1	
CMD28	A4 BA2	
CMD29	A2 BA0	
CMD30	A3 BA3	
CMD31		



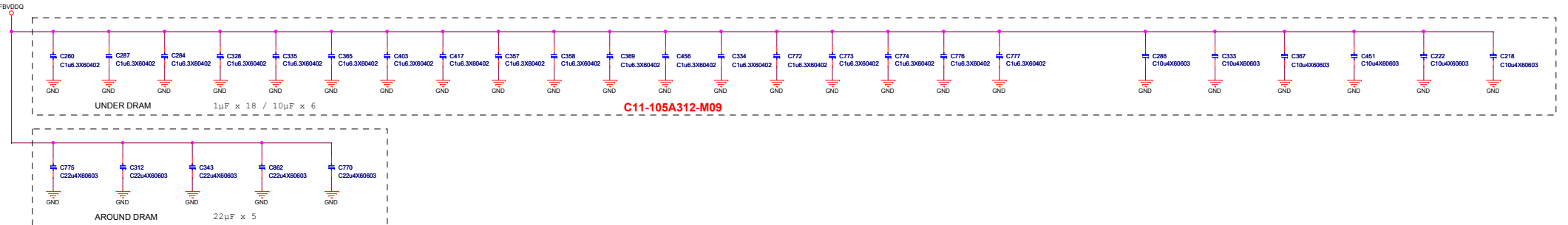
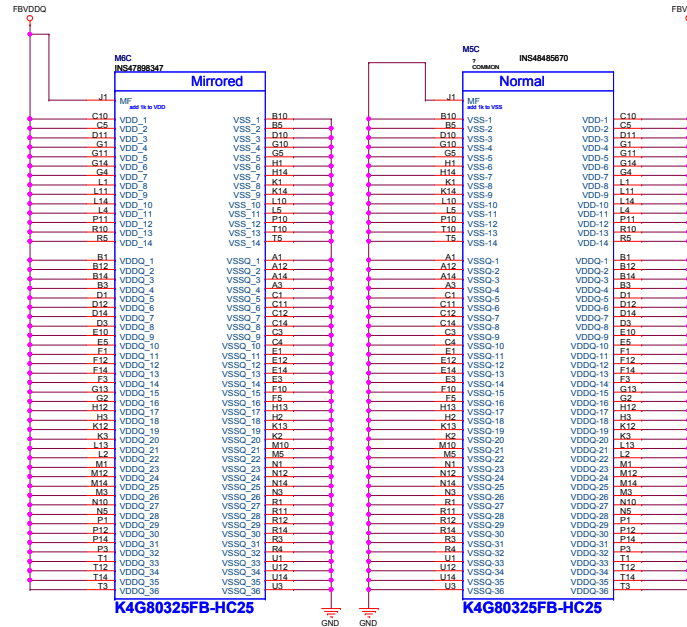
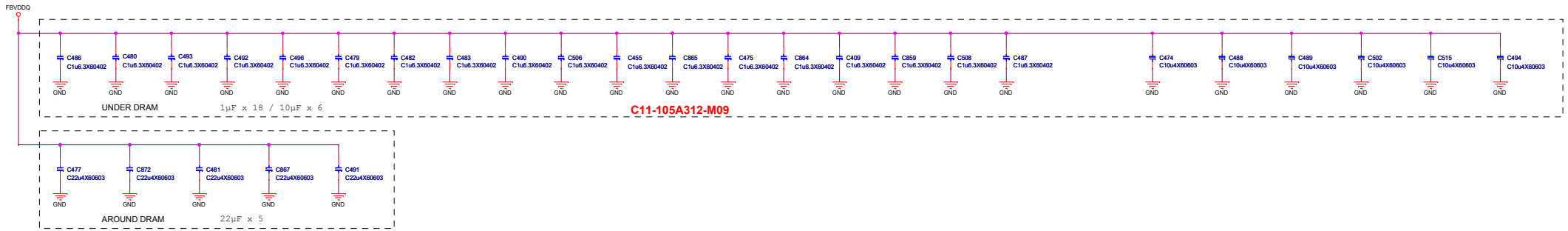
DGPU_GDDR5 FrameBuffer C0



DGPU_GDDR5 FrameBuffer C1



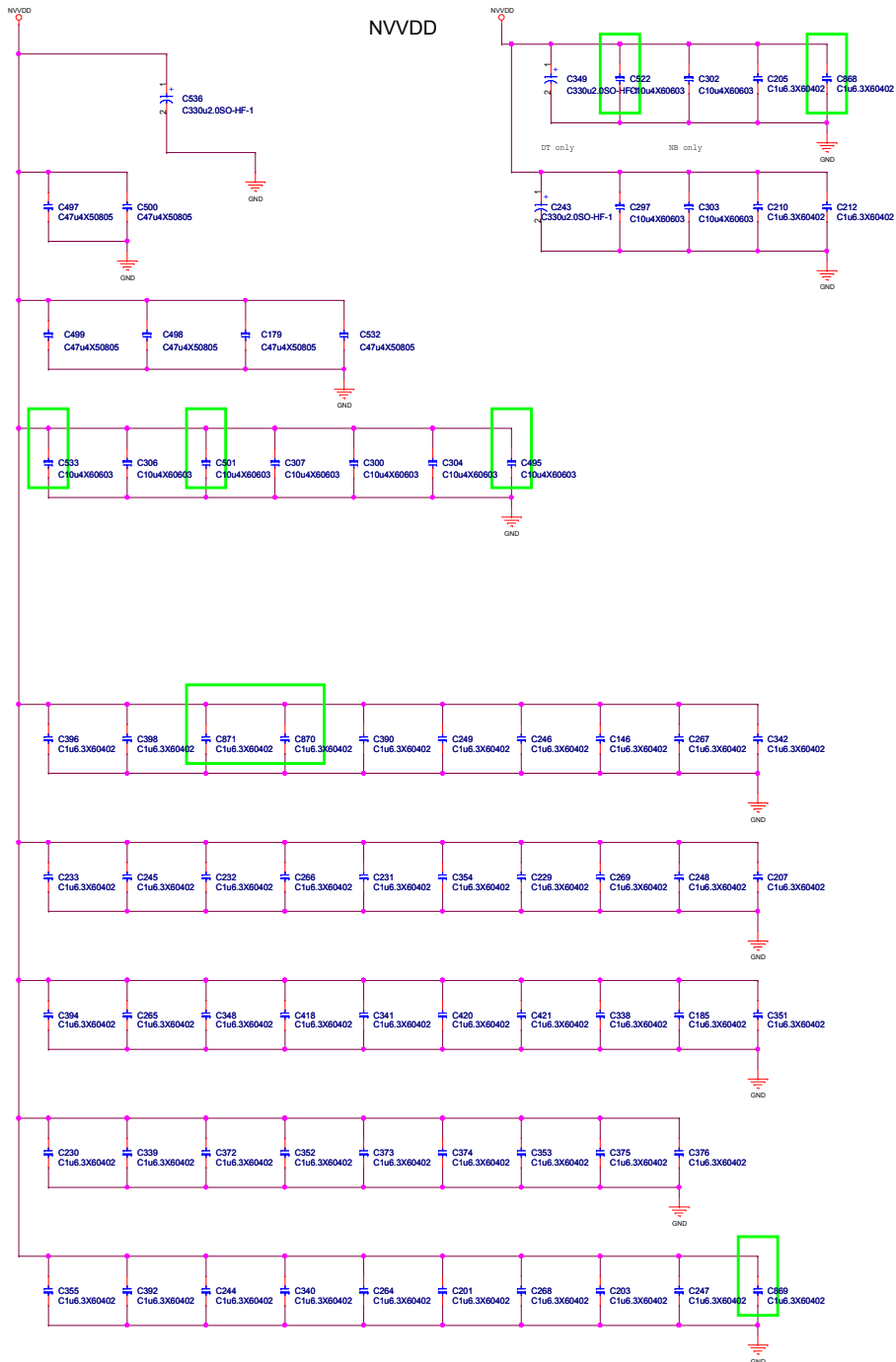
Frame Buffer Partition C Decoupling



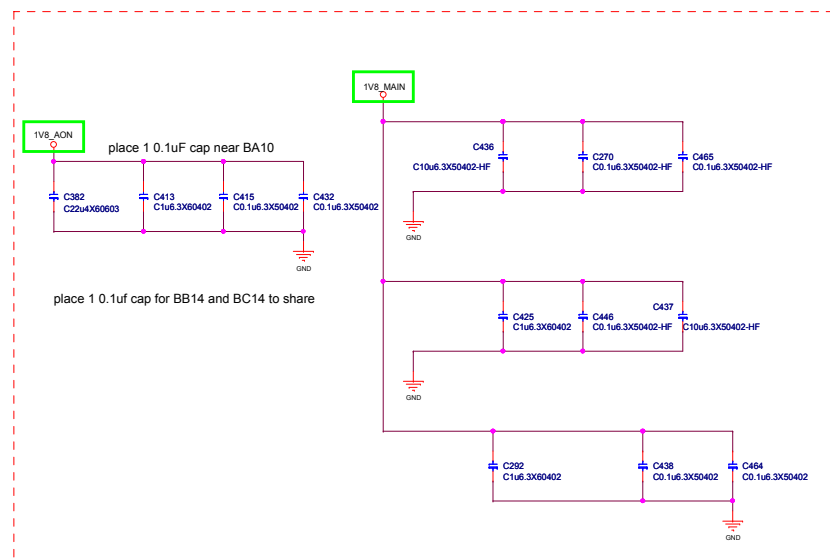
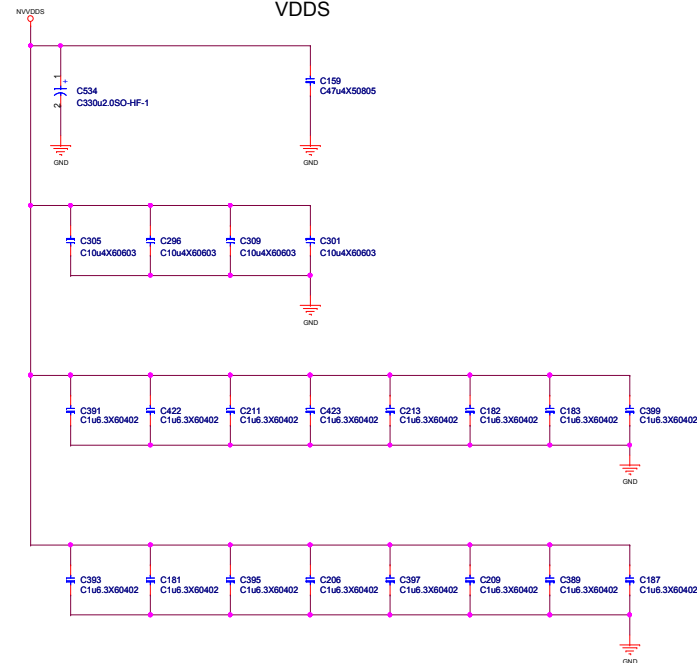
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Samsung PN : M12-8032535-S02 / K4G80325FB-HC25 (256Mx32bit)

GPU DECOUPLING A

NVVD



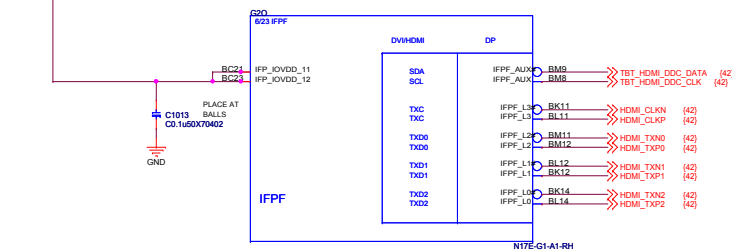
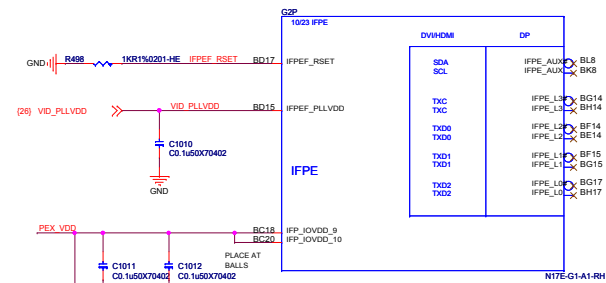
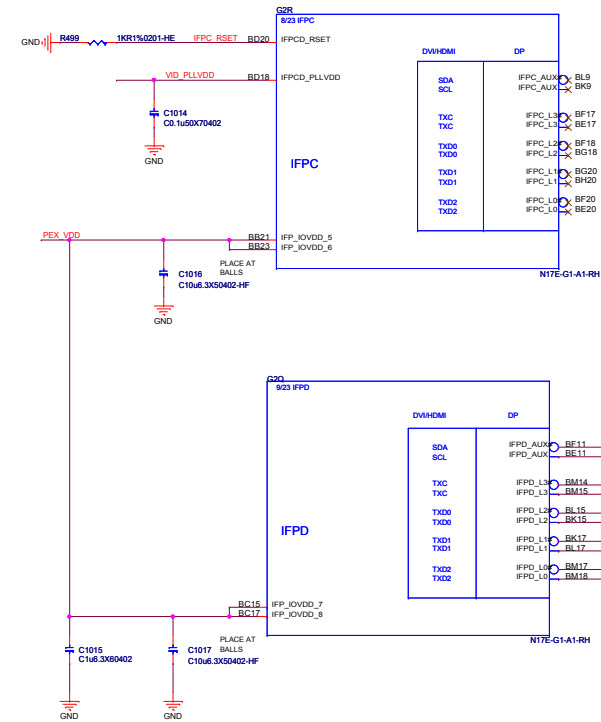
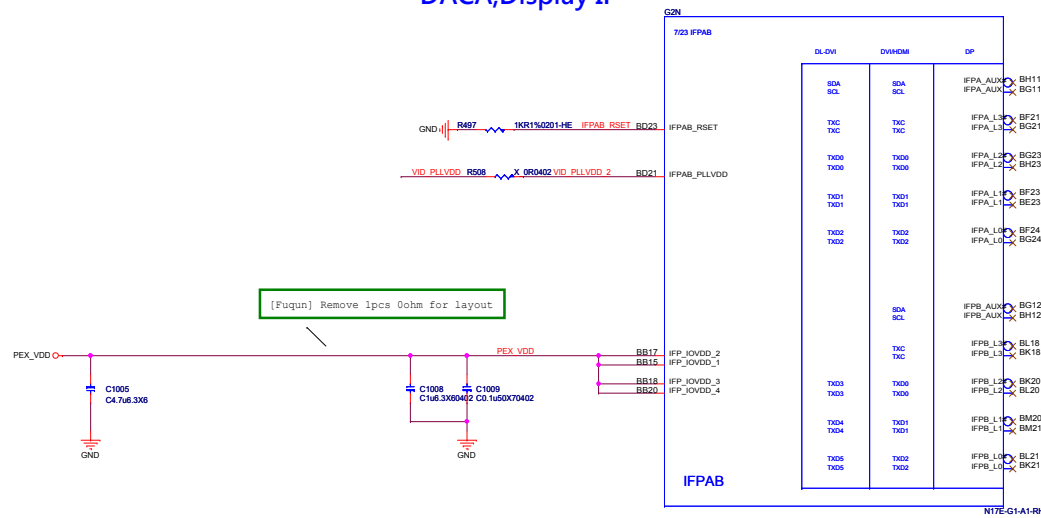
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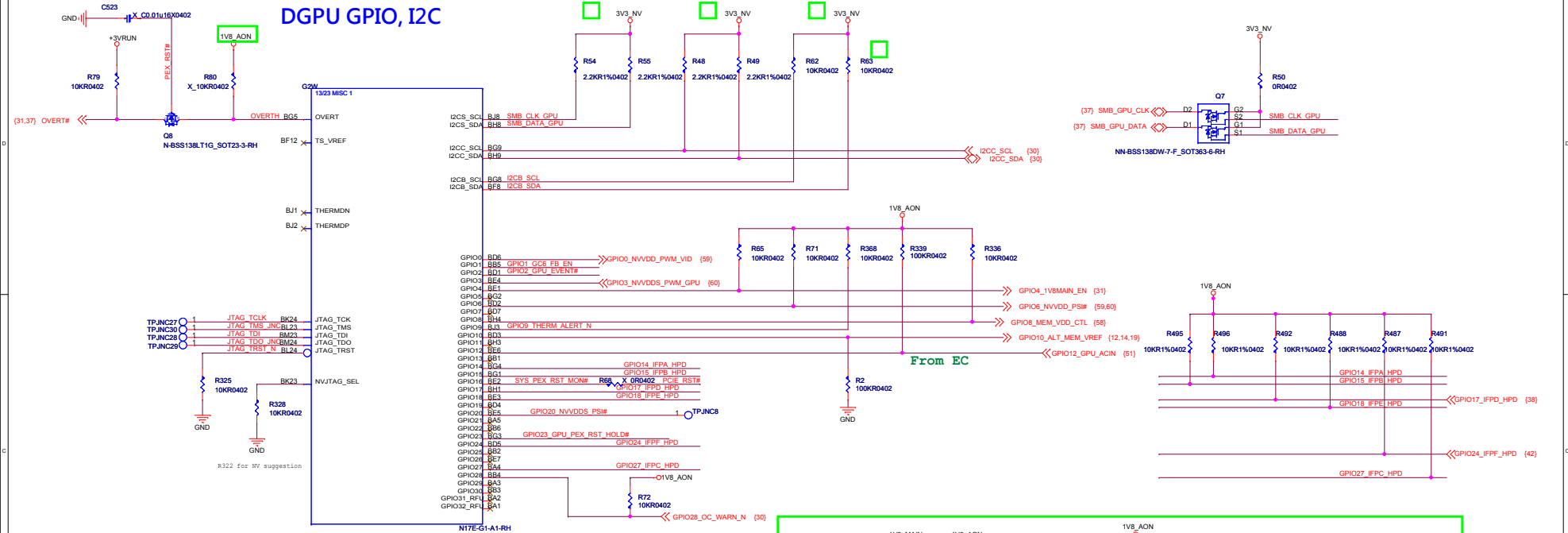
GPU DECOUPLING B



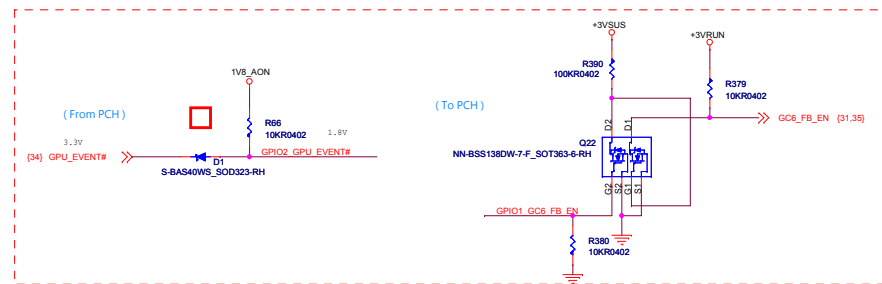
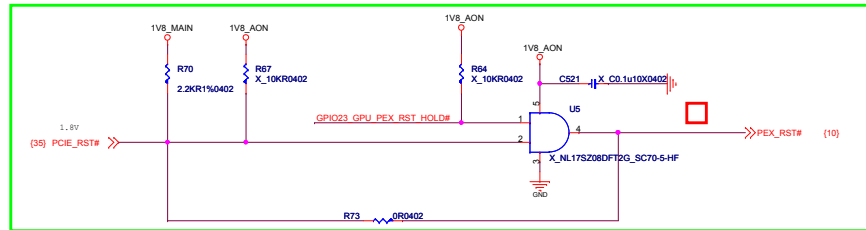
DACA,Display IF



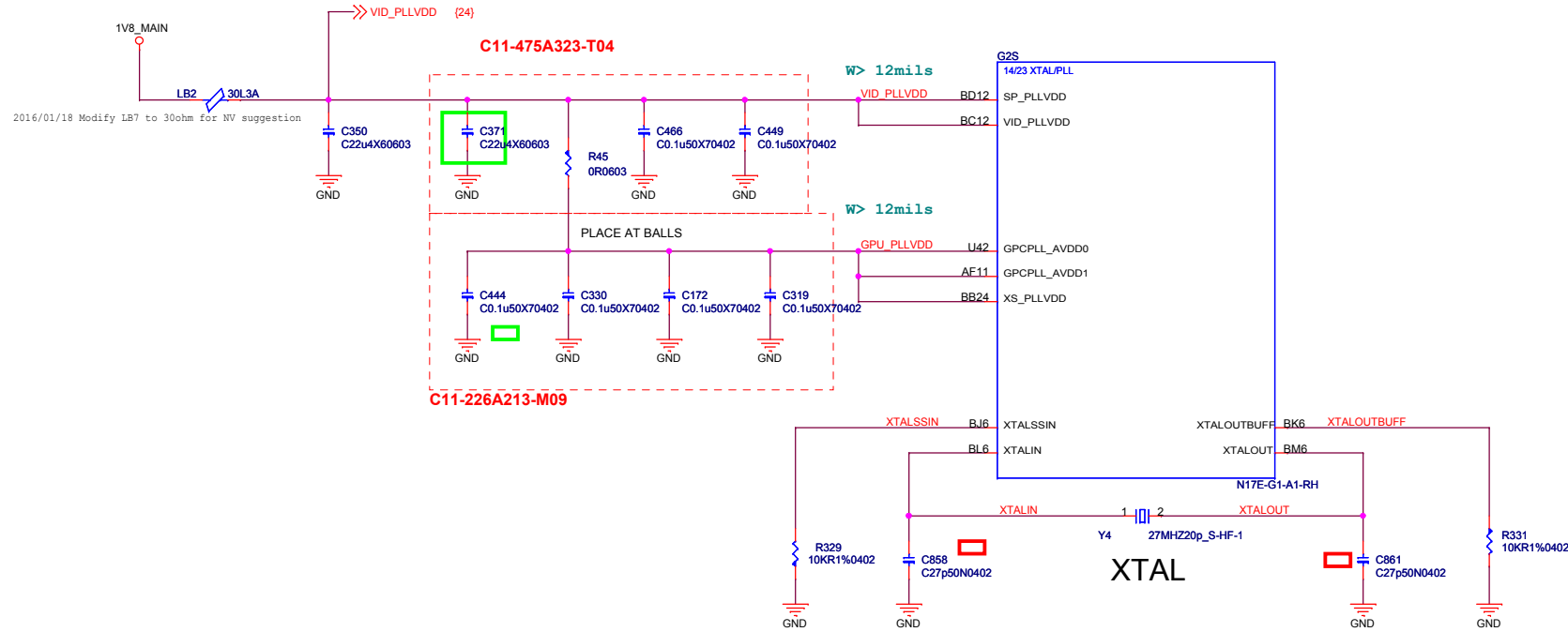
DGPU GPIO, I2C



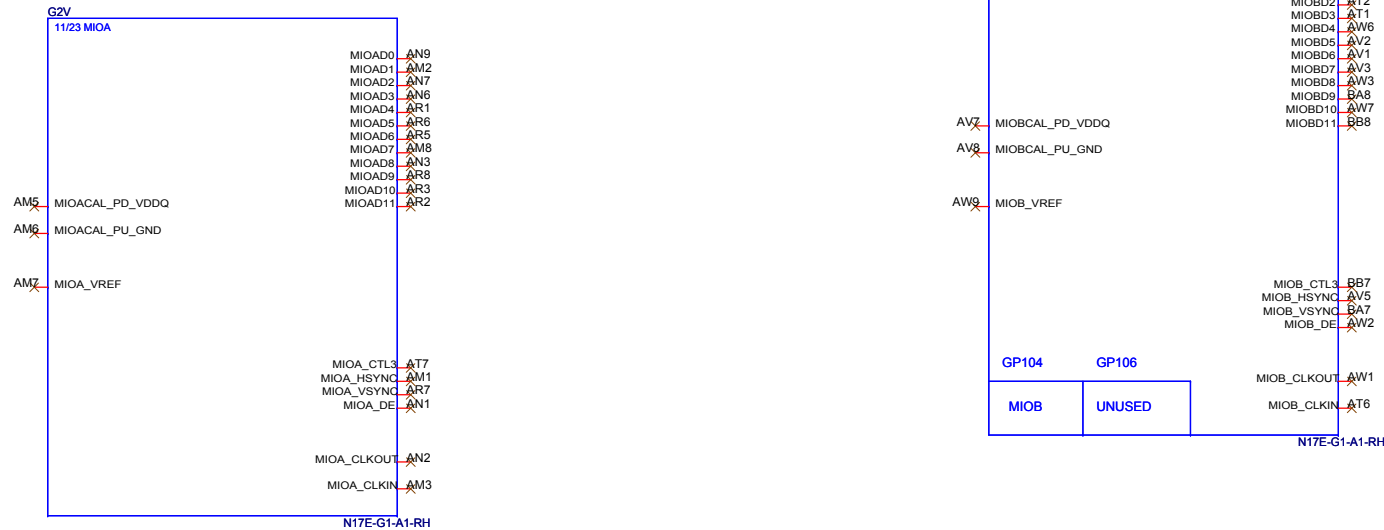
Pin Name	Normal function	I/O	Functional Description	Recommended Default Pull-up or Pull-down
GPIO0	FWR_VID	O	GPU Core VDD PWM control signal	0 to 1V8 FWM output
GPIO1	GC6_FB_EN	O	FB Enable for GC6 2.1	10K pull-down
GPIO2	GPU_EVENT#	I	GPU wake signal for GC6 2.1	10K pull-up to 1V8 _AON
GPIO3	NVVDD_SRAM_PWM	O	PWM output to control the SRAM power supply	10K pull-down
GPIO4	1V8_MAIN_EN	O	GPU POWER Sequencing for GC6 2.1	10K pull-up to 1V8 _AON
GPIO5	FRM_LCK	I	Active low Fram Lock	1V8 pull-up to 1V8 _AON
GPIO6	PSI	O	Phase shedding	10K pull-up to 1V8 _AON
GPIO7	LCD_BI_PWM	O	Panel Backlight PWM Brightness Control	100K pull-down
GPIO8	MEM_VDD_CTL	O	Memory Voltage Control	pull-up/pull-down to set the revsio/g power-on voltage
GPIO9	THERM_ALERT	I/O	Active Low Thermal Alert	10K pull-up to 1V8 _AON
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100K pull-down
GPIO11	LCD_VCC	O	Panel Power Enable	100K pull-down
GPIO12	FWR_LEVEL	I	AC power detect or power supply overdraw input	100K pull-up to 1V8 _AON
GPIO13	LCD_BLEN	O	Panel Backlight Enable	100K pull-down
GPIO14	HPD_A	I	Hot Plug Detect for IFPA	
GPIO15	HPD_B	I	Hot Plug Detect for IFPB	
GPIO16	SYS_PEX_RST_MON#	I	System side PCI reset Monitor	10K pull-up to 3V3 _AON
GPIO17	HPD_D	I	Hot Plug Detect for IFPD	
GPIO18	HPD_E	I	Hot Plug Detect for IFPE	
GPIO19	3Dvision	O	3D Vision L/R signal	100K pull-down
GPIO20	NVVDDS_PSI GC5_MODE	O		
GPIO21	SLI_RASTER_SYNC	I	SLI Raster Sync	100K pull-down
GPIO22	SLI_SWAP_DRY	I	SLI Swap Ready	1K pull-up to 3V3 _AON
GPIO23	GPU_PEX_RST_HOLD	O	GPU PCIe self-reset control	10K pull-up to 3V3
GPIO24	HPD_F	I	Hot Plug Detect for IFPDF	
GPIO25	RESERVED			
GPIO26	RESERVED			
GPIO27	HPD_C	I	Hot Plug Detect for IFPC	
GPIO28	OC_WARN	I	Over current throttling	10K pull-up to 1V8 _AON
GPIO29	EDPo_OUTPUT_CAP	I	Input from power supply	0 to 1V8
GPIO30	RESERVED			



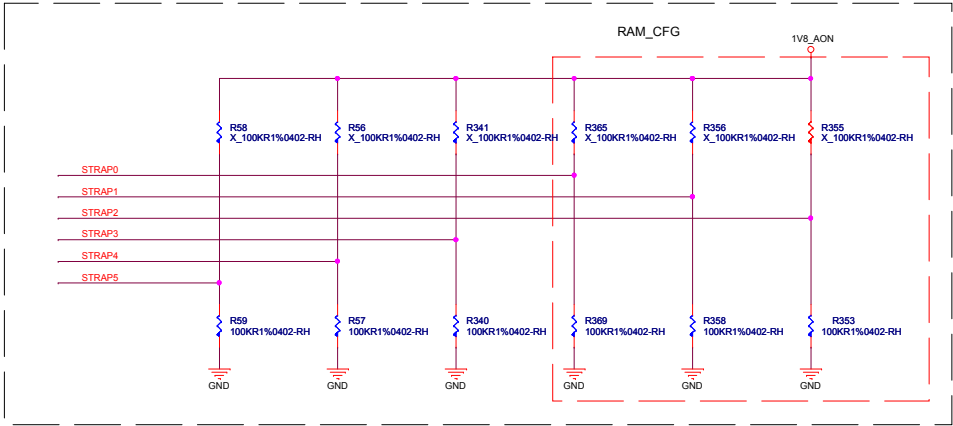
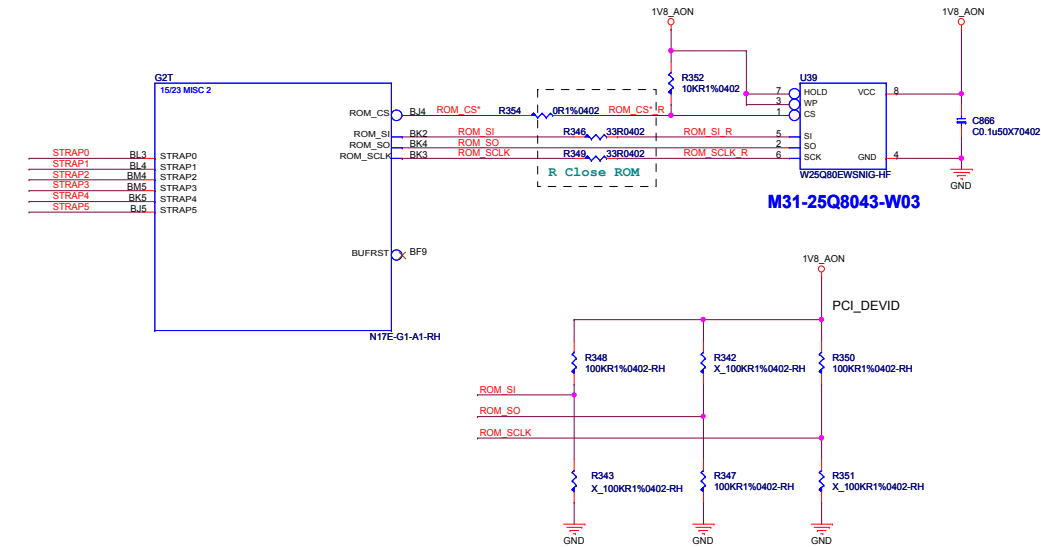
DGPU MIO & XTAL



Multi-use IO(MIO) Interface



ROM, MULTI-LEVEL STRAPS



V_TOP1	5010
DEFAULT SETTING	M12-8032535-S02
	X_K4G80325FB-HC25
V_TOP2	5010
	M12-2563215-M30
	X_MT51J256M32HF-80-A
V_TOP3	5010
	M12-5GC2H05-H23
	X_H5GC2H24BFR-T2C

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	00000	V
L	L	H	00001	V
L	H	L	00010	
L	H	H	00011	
H	H	L	00110	
H	H	H	00111	

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

SAMSUNG 0X0
MICRON 0X1
HYNIX 0X2

ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]	1:ENABLE 0:DISABLE
L	L	L	1111 DEFAULT	SOR0/1/2/3 ENABLE
L	L	H	1110	
L	H	L	1101	
L	H	H	1100	
H	L	L	1011	
H	L	H	1010	
H	H	L	1001	
H	H	H	1000	
L	L	M	0111	
L	M	L	0110	
L	M	H	0101	
L	H	M	0100	
H	L	M	0011	
H	M	L	0010	
H	M	H	0001	
H	H	M	0000	V

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0 V

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

DGPU GND

G2M
N17E-G1-A1-RH

GND

GND

G2K
N17E-G1-A1-RH

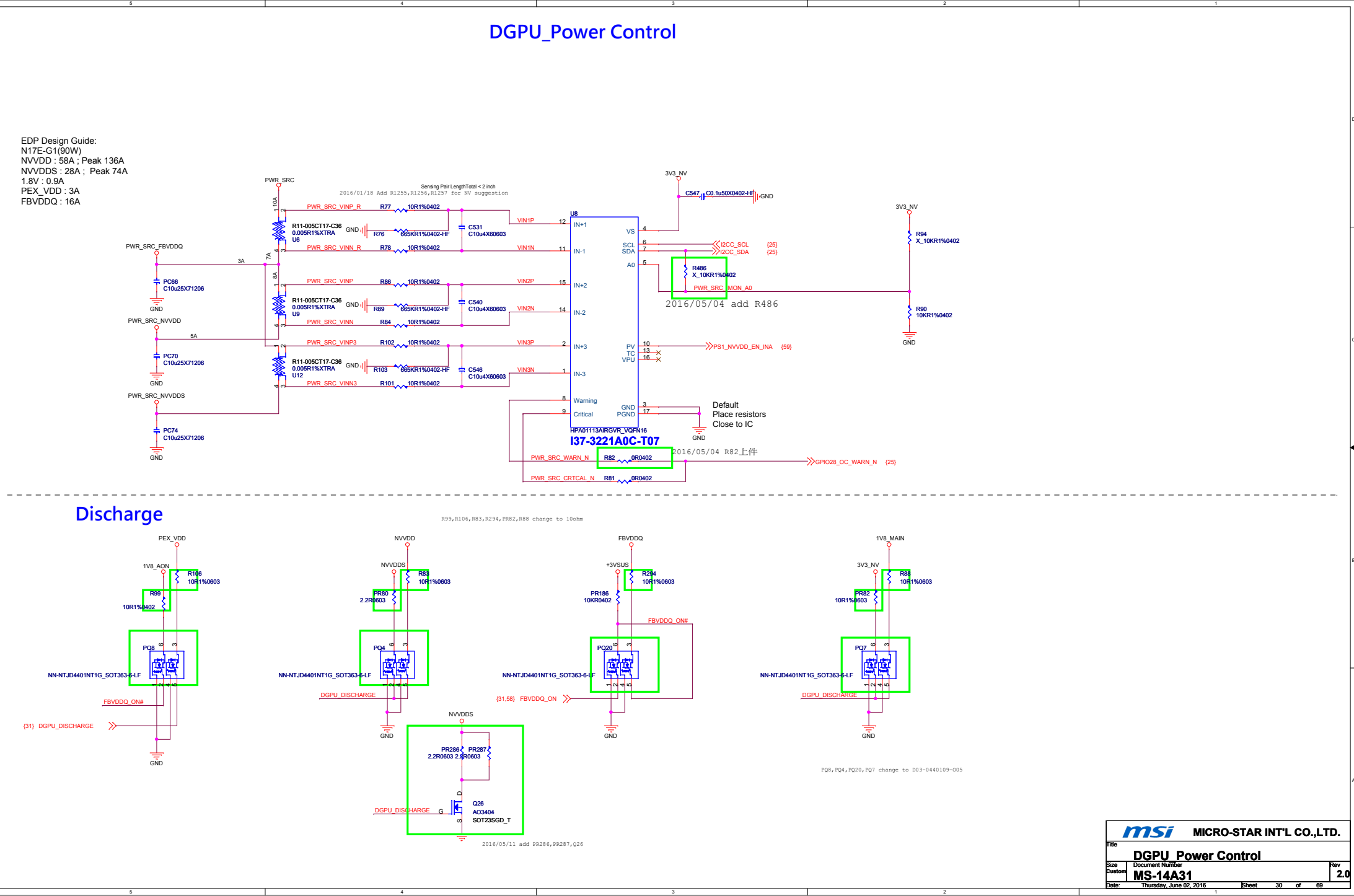
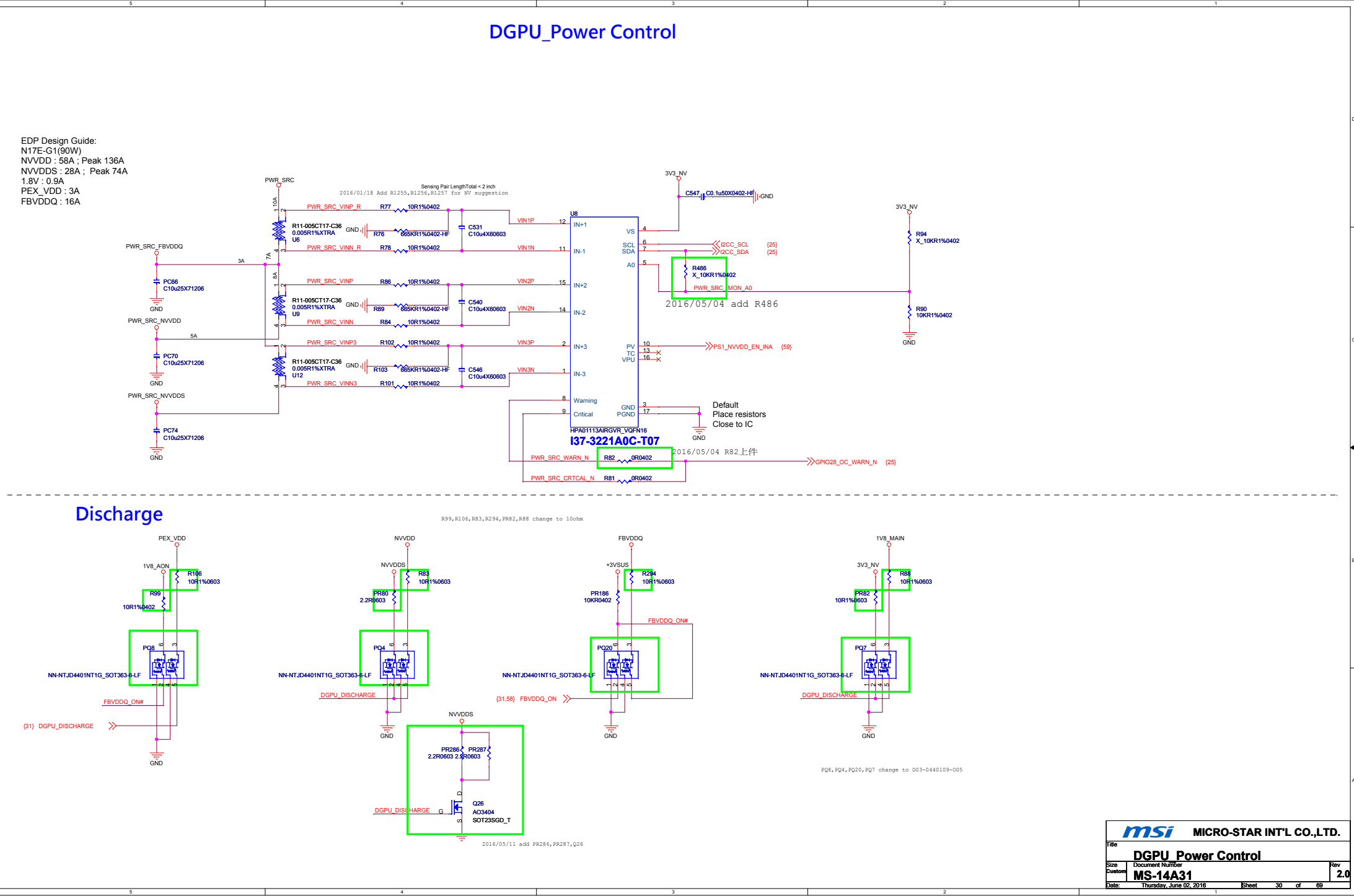
GND

GND

G2L
N17E-G1-A1-RH

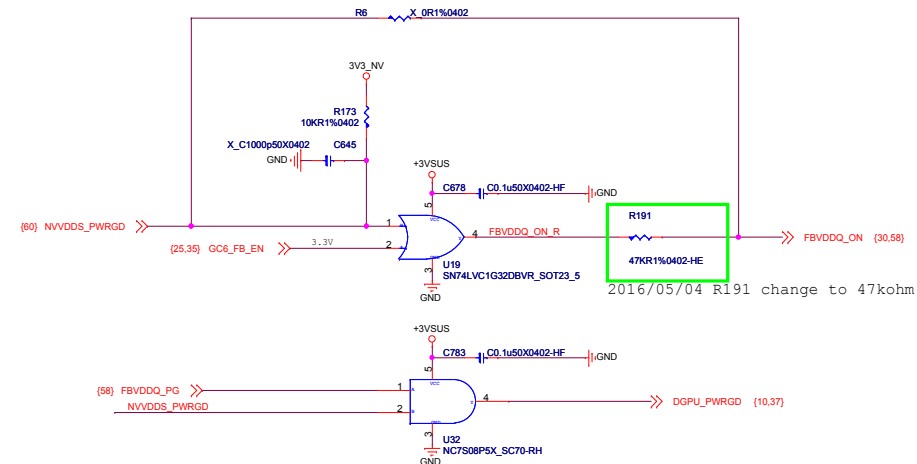
GND

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BL47	GND_486	GND_490
BL48	GND_487	GND_491
BL49	GND_488	GND_492
BL50	GND_489	GND_493
BL51	GND_490	GND_494
BL52	GND_491	GND_495
BL53	GND_492	GND_496
BL54	GND_493	GND_497
BL55	GND_494	GND_498
BL56	GND_495	GND_499
BL57	GND_496	GND_500
BL58	GND_497	GND_501
BL59	GND_498	GND_502
BL60	GND_499	GND_503
BL61	GND_500	GND_504
BL62	GND_501	GND_505
BL63	GND_502	GND_506
BL64	GND_503	GND_507
BL65	GND_504	GND_508
BL66	GND_505	GND_509
BL67	GND_506	GND_510
BL68	GND_507	GND_511
BL69	GND_508	GND_512
BL70	GND_509	GND_513
BL71	GND_510	GND_514
BL72	GND_511	GND_515
BL73	GND_512	GND_516
BL74	GND_513	GND_517
BL75	GND_514	GND_518
BL76	GND_515	GND_519
BL77	GND_516	GND_520
BL78	GND_517	GND_521
BL79	GND_518	GND_522
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BL83	GND_522	GND_526
BL84	GND_523	GND_527
BL85	GND_524	GND_528
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BL89	GND_528	GND_532
BL90	GND_529	GND_533
BL91	GND_530	GND_534
BL92	GND_531	GND_535
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BL94	GND_533	GND_537
BL95	GND_534	GND_538
BL96	GND_535	GND_539
BL97	GND_536	GND_540
BL98	GND_537	GND_541
BL99	GND_538	GND_542
BL00	GND_539	GND_543
BL01	GND_540	GND_544
BL02	GND_541	GND_545
BL03	GND_542	GND_546
BL04	GND_543	GND_547
BL05	GND_544	GND_548
BL06	GND_545	GND_549
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BL08	GND_547	GND_551
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BL10	GND_549	GND_553
BL11	GND_550	GND_554
BL12	GND_551	GND_555
BL13	GND_552	GND_556
BL14	GND_553	GND_557
BL15	GND_554	GND_558
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BL20	GND_559	GND_563
BL21	GND_560	GND_564
BL22	GND_561	GND_565
BL23	GND_562	GND_566
BL24	GND_563	GND_567
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BL27	GND_566	GND_570
BL28	GND_567	GND_571
BL29	GND_568	GND_572
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BL34	GND_573	GND_577
BL35	GND_574	GND_578
BL36	GND_575	GND_579
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BL89	GND_628	GND_632
BL90	GND_629	GND_633
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BL13	GND_852	GND_856

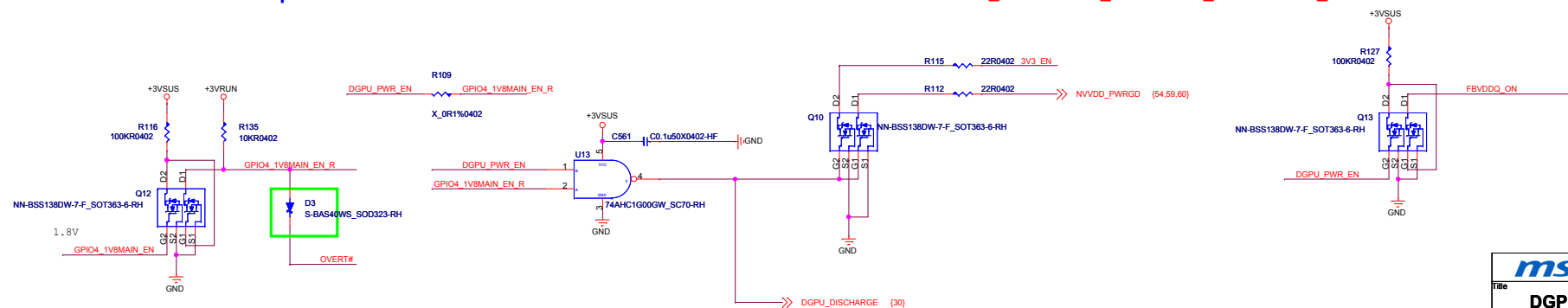
[illegible][illegible][illegible]

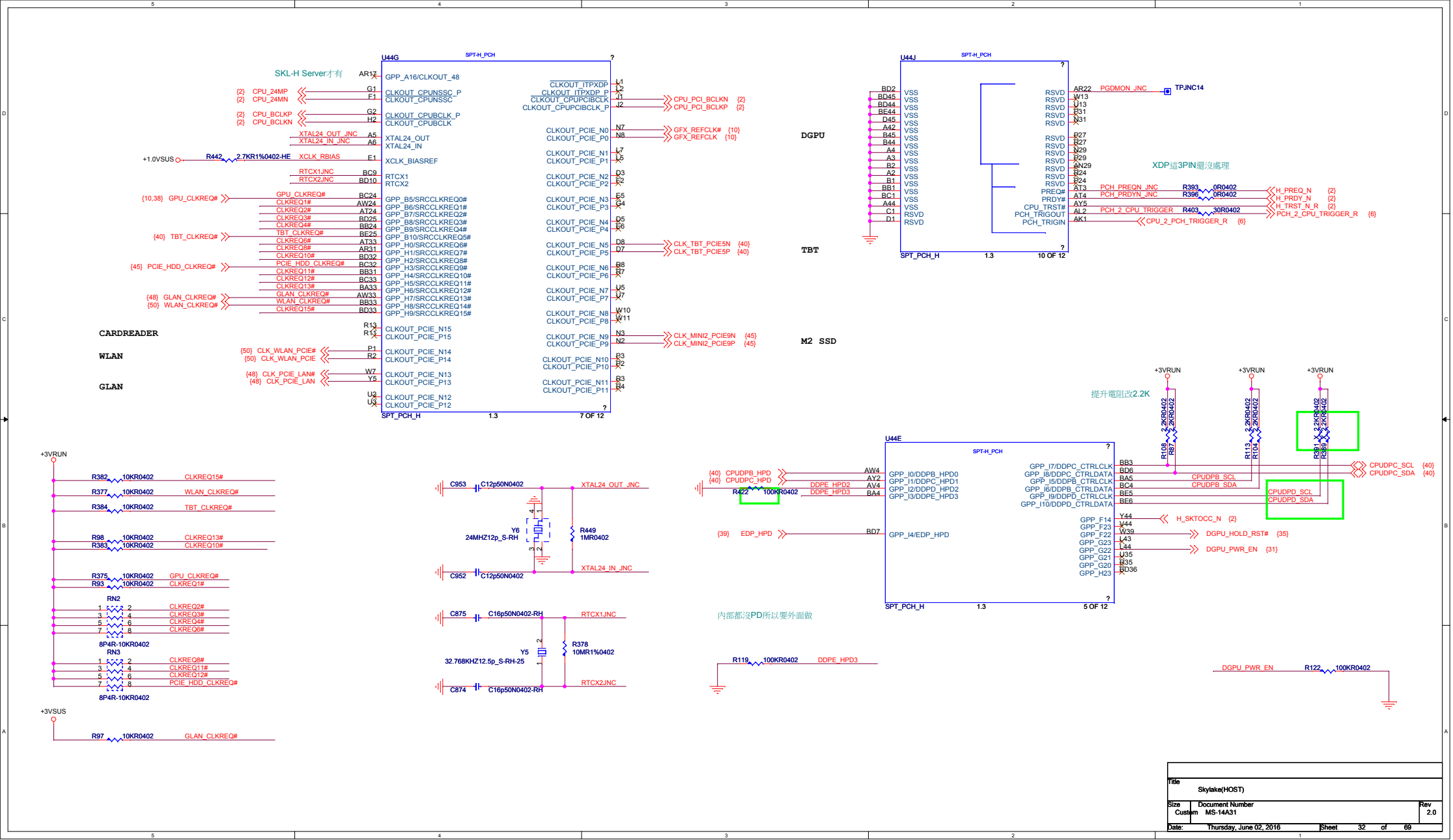
1V8_AON

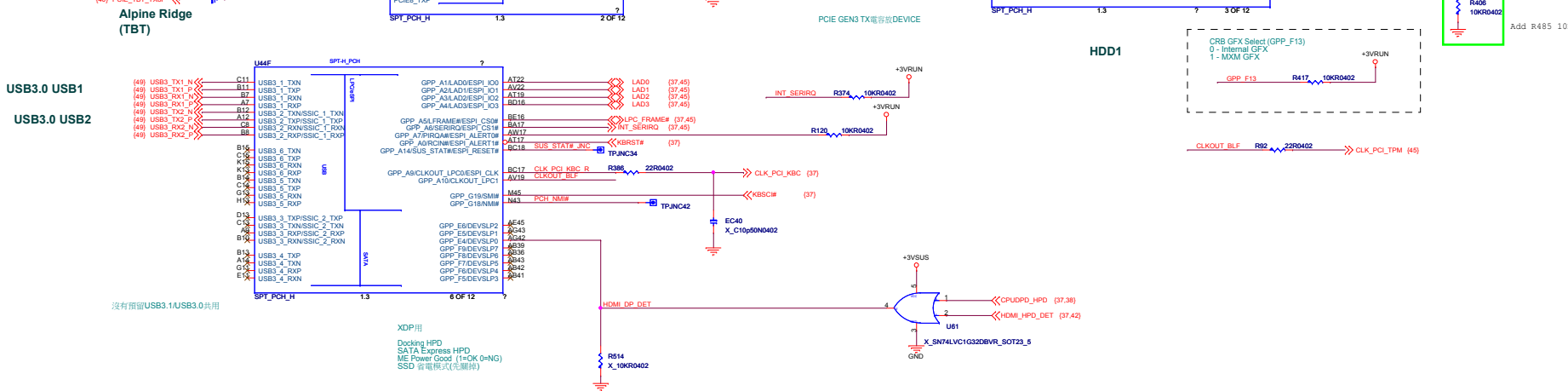
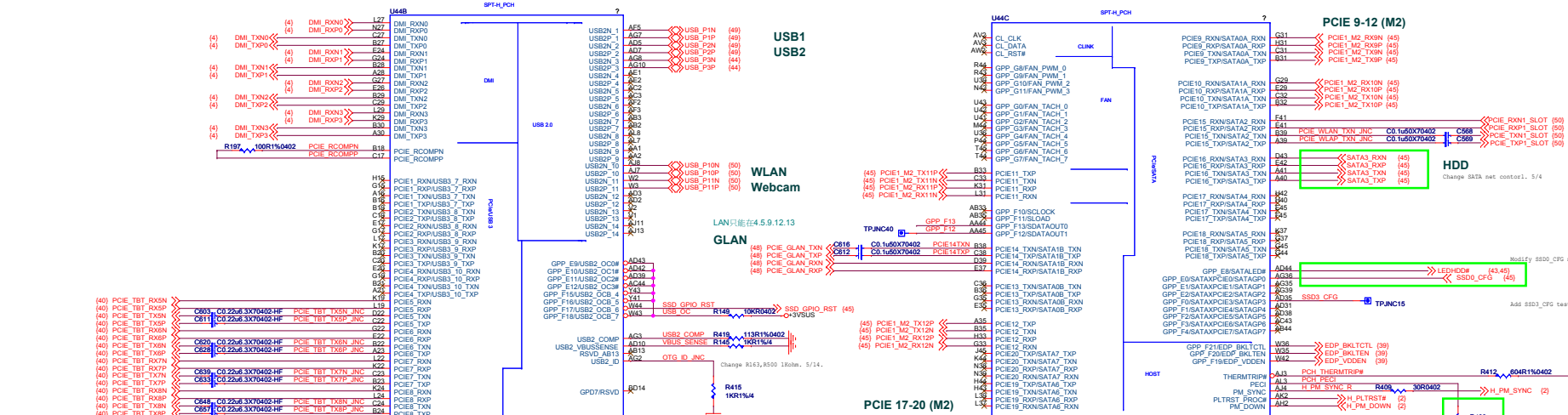
2016/05/04 Add R485, D12



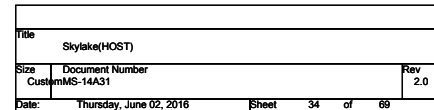
Power down = FBVDDQ -> NVDDS/PEX_VDD -> 3V3_NV -> 1V8_AON -> 1V8_MAIN

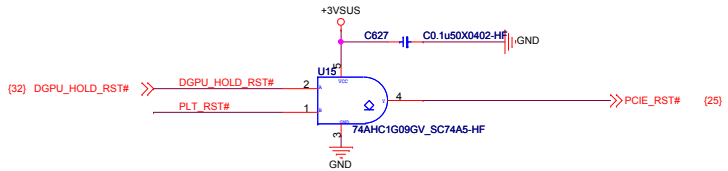
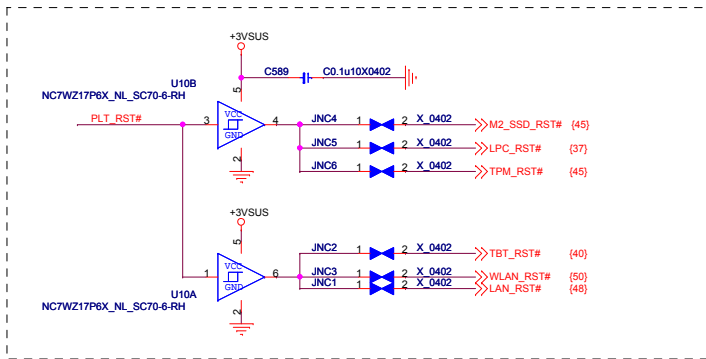
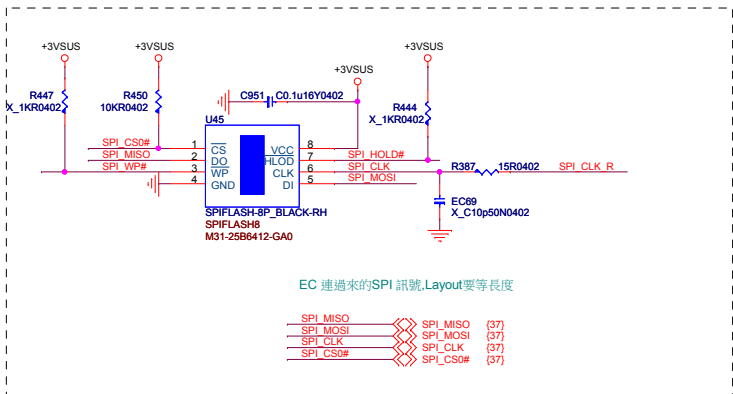
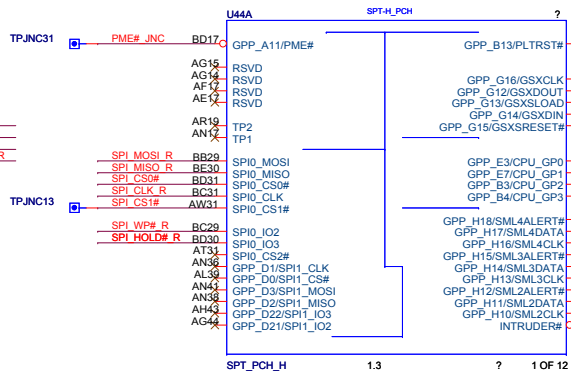
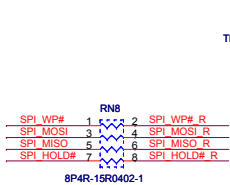


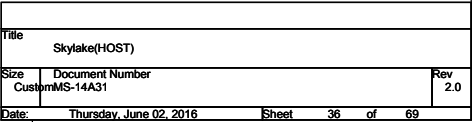




PCH EDS Page 52

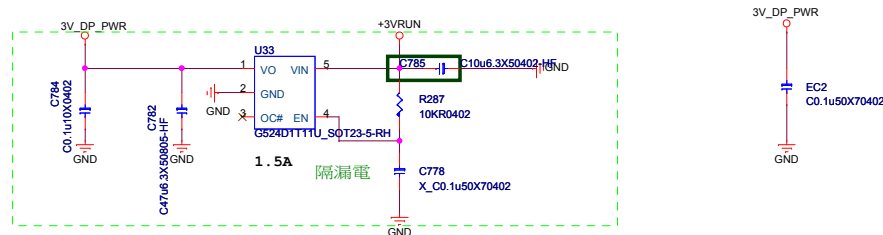




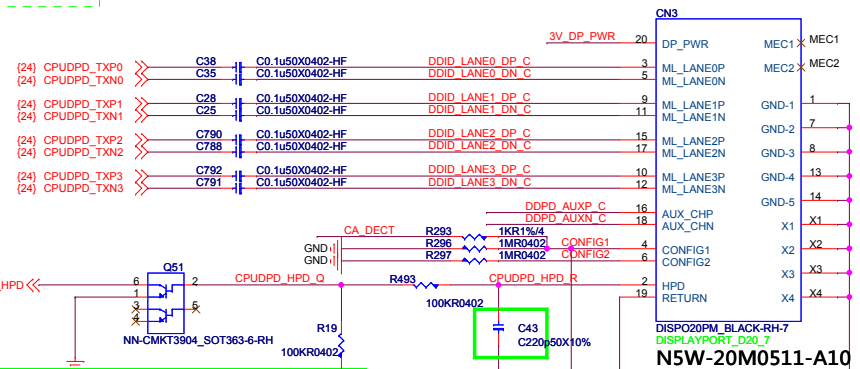


Display Port

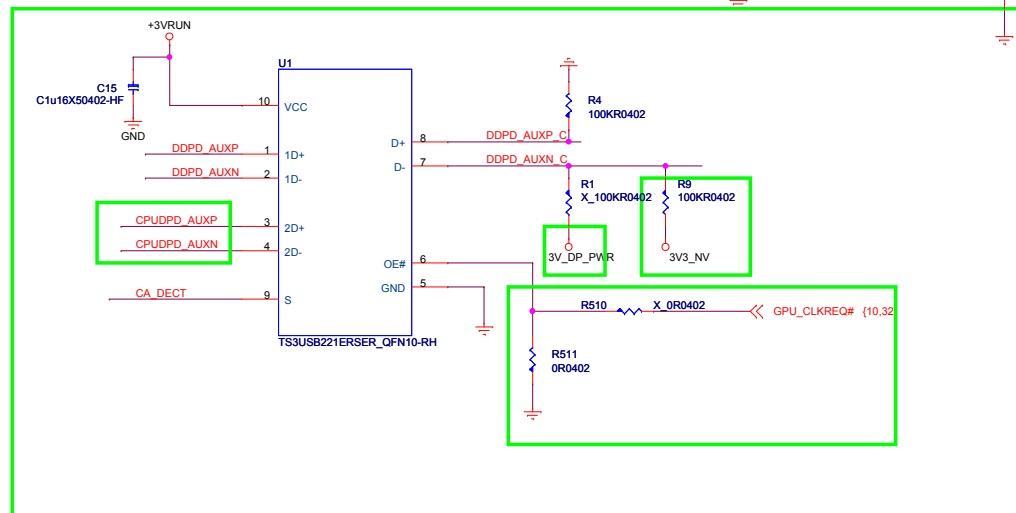
The preset trip limit must not exceed 3A at the Upstream device connector DP_PWR pin and 1.5A at the Downstream device connector DP_PWR pin.



Display Port

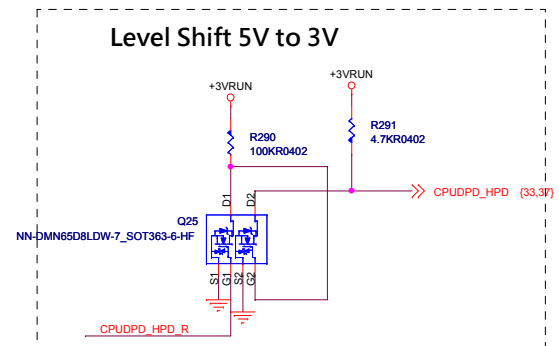


DP/TMDS mode select



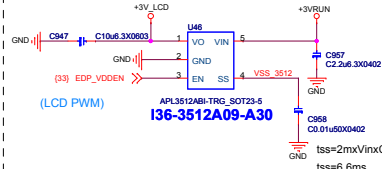
TS3USB221A TRUTH TABLE

S	OE#	FUNCTION
X	H	Disconnect
L	L	D = 1D
H	L	D = 2D

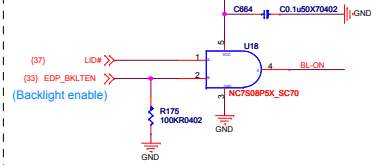


eDP Connector

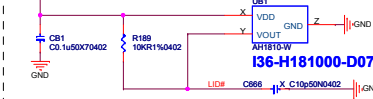
Panel Device Logic Power



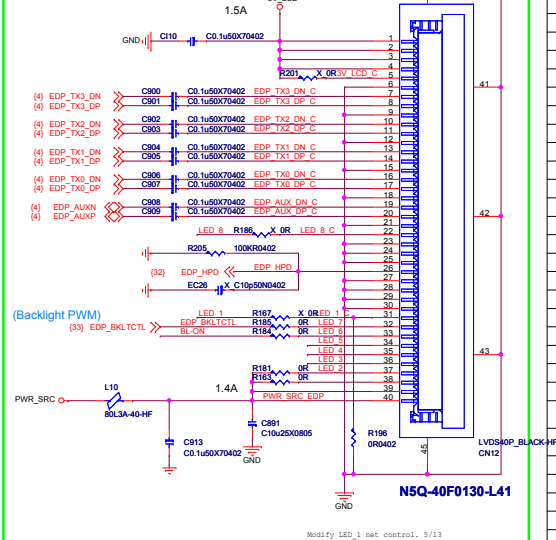
Backlight



Hall Switch



eDP CONN



LCD Module Pin Define FOR FULL HD PANEL

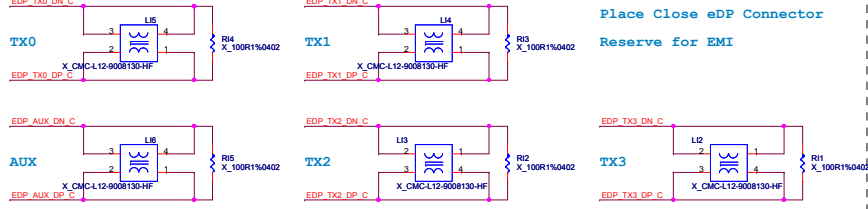
Pin No	Symbol	Description
1	Vcom SDA	Vcom IIC SDA
2	H_GND	High Speed Ground
3	LAN1_N	Complement Signal-Lane 1
4	LAN1_P	True Signal-Main Lane 1
5	H_GND	High Speed Ground
6	LAN0_N	Complement Signal-Lane 0
7	LAN0_P	True Signal-Main Lane 0
8	H_GND	High Speed Ground
9	AUX+	True Signal-Auxiliary Channel
10	AUX-	Complement Signal-Auxiliary Channel
11	H_GND	High Speed Ground
12	LCD_VCC	Power Supply +3.3 V (typical)
13	LCD_VCC	Power Supply +3.3 V (typical)
14	NC	No Connection (Reserved for CMI test)
15	H_GND	Ground
16	H_GND	Ground
17	HPD	Hot Plug Detect
18	BL_GND	BL Ground
19	BL_GND	BL Ground
20	BL_GND	BL Ground
21	BL_GND	BL Ground
22	BL_EN	BL_Enable Signal of LED Converter
23	BL_PWM	PWM Dimming Control Signal of LED Converter
24	Vcom SCL	Vcom IIC SCL
25	NC	No Connection (Reserved)
26	LED_VCCS	BL Power
27	LED_VCCS	BL Power
28	LED_VCCS	BL Power
29	LED_VCCS	BL Power
30	NC	No Connection (Reserved)

LCD Module Pin Define FOR WQHD PANEL

Pin No	Symbol	Description
1	NC	Reserved for LCD manufacturer's use
2	H_GND	High Speed Ground
3	Lane3_N	Complement Signal Link Lane 3
4	Lane3_P	True Signal Link Lane 3
5	H_GND	High Speed Ground
6	Lane2_N	Complement Signal Link Lane 2
7	Lane2_P	True Signal Link Lane 2
8	H_GND	High Speed Ground
9	Lane1_N	Complement Signal Link Lane 1
10	Lane1_P	True Signal Link Lane 1
11	H_GND	High Speed Ground
12	Lane0_N	Complement Signal Link Lane 0
13	Lane0_P	True Signal Link Lane 0
14	H_GND	High Speed Ground
15	AUX_CH_P	True Signal Auxiliary Channel
16	AUX_CH_N	Complement Signal Auxiliary Channel
17	H_GND	High Speed Ground
18	VDD	LCD logic and driver power(3.3V)
19	VDD	LCD logic and driver power(3.3V)
20	VDD	LCD logic and driver power(3.3V)
21	VDD	LCD logic and driver power(3.3V)
22	BIST	BIST patterns selection L : Disable (default) , H : Enable
23	LCD_GND	LCD logic and driver ground
24	LCD_GND	LCD logic and driver ground
25	LCD_GND	LCD logic and driver ground
26	LCD_GND	LCD logic and driver ground
27	HPD	HPD signal pin
28	BL_GND	Backlight ground
29	BL_GND	Backlight ground
30	BL_GND	Backlight ground
31	BL_GND	Backlight ground
32	BL_ENABLE	Backlight On/off
33	BL_PWM_DIM	System PWM
34	NC	Reserved for LCD manufacturer's use
35	NC	Reserved for LCD manufacturer's use
36	VBL	Backlight power
37	VBL	Backlight power
38	VBL	Backlight power
39	VBL	Backlight power
40	NC	No Connection (Reserved)

LCD Module Pin Define FOR QHD+ PANEL

Pin No	Symbol	Description
1	NC	Reserved for LCD manufacturer's use
2	H_GND	High Speed Ground
3	Lane3_N	Complement Signal Link Lane 3
4	Lane3_P	True Signal Link Lane 3
5	H_GND	High Speed Ground
6	Lane2_N	Complement Signal Link Lane 2
7	Lane2_P	True Signal Link Lane 2
8	H_GND	High Speed Ground
9	Lane1_N	Complement Signal Link Lane 1
10	Lane1_P	True Signal Link Lane 1
11	H_GND	High Speed Ground
12	Lane0_N	Complement Signal Link Lane 0
13	Lane0_P	True Signal Link Lane 0
14	H_GND	High Speed Ground
15	AUX_CH_P	True Signal Auxiliary Channel
16	AUX_CH_N	Complement Signal Auxiliary Channel
17	H_GND	High Speed Ground
18	NC	Reserved for LCD manufacturer's use
19	NC	Reserved for LCD manufacturer's use
20	VDD	LCD logic and driver power(3.3V)
21	VDD	LCD logic and driver power(3.3V)
22	VDD	LCD logic and driver power(3.3V)
23	VDD	LCD logic and driver power(3.3V)
24	VDD	LCD logic and driver power(3.3V)
25	NC	Reserved for LCD manufacturer's use
26	LCD_GND	LCD logic and driver ground
27	LCD_GND	LCD logic and driver ground
28	LCD_GND	LCD logic and driver ground
29	LCD_GND	LCD logic and driver ground
30	LCD_GND	LCD logic and driver ground
31	HPD	Backlight ground
32	NC	Reserved for LCD manufacturer's use
33	PWM_OUT	PWM_OUT
34	PWM_IN	PWM_IN
35	NC	Reserved for LCD manufacturer's use
36	NC	Reserved for LCD manufacturer's use
37	NC	Reserved for LCD manufacturer's use
38	VBL	LED Anode
39	VBL	LED Anode
40	NC	Reserved for LCD manufacturer's use
41	LED_C1	LED Cathode 1
42	LED_C2	LED Cathode 2
43	LED_C3	LED Cathode 3
44	LED_C4	LED Cathode 4
45	LED_C5	LED Cathode 5
46	LED_C6	LED Cathode 6
47	LED_C7	LED Cathode 7
48	LED_C8	LED Cathode 8
49	NC	Reserved for LCD manufacturer's use
50	NC	Reserved for LCD manufacturer's use

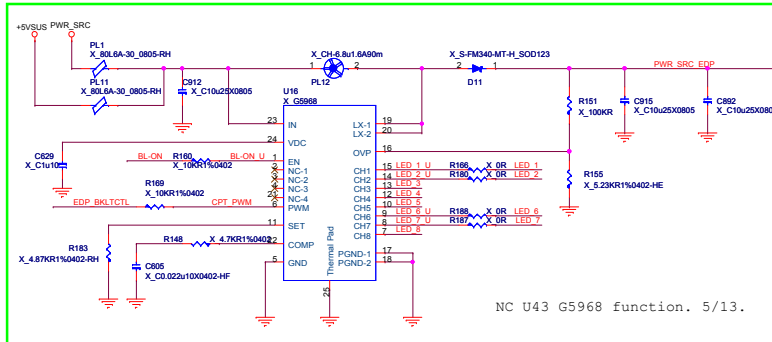


Place Close eDP Connector

Reserve for EMI

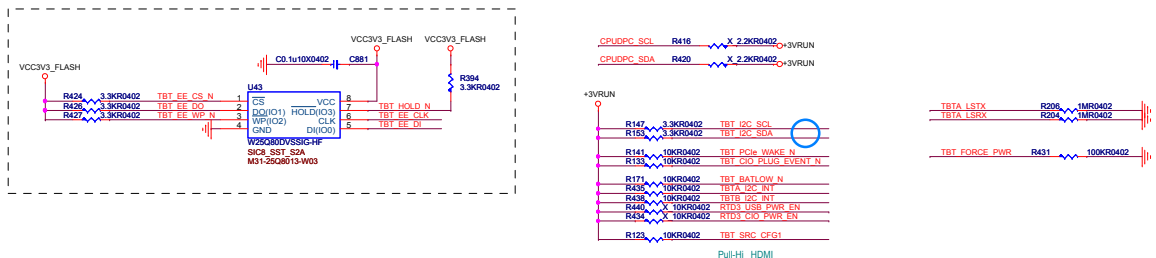
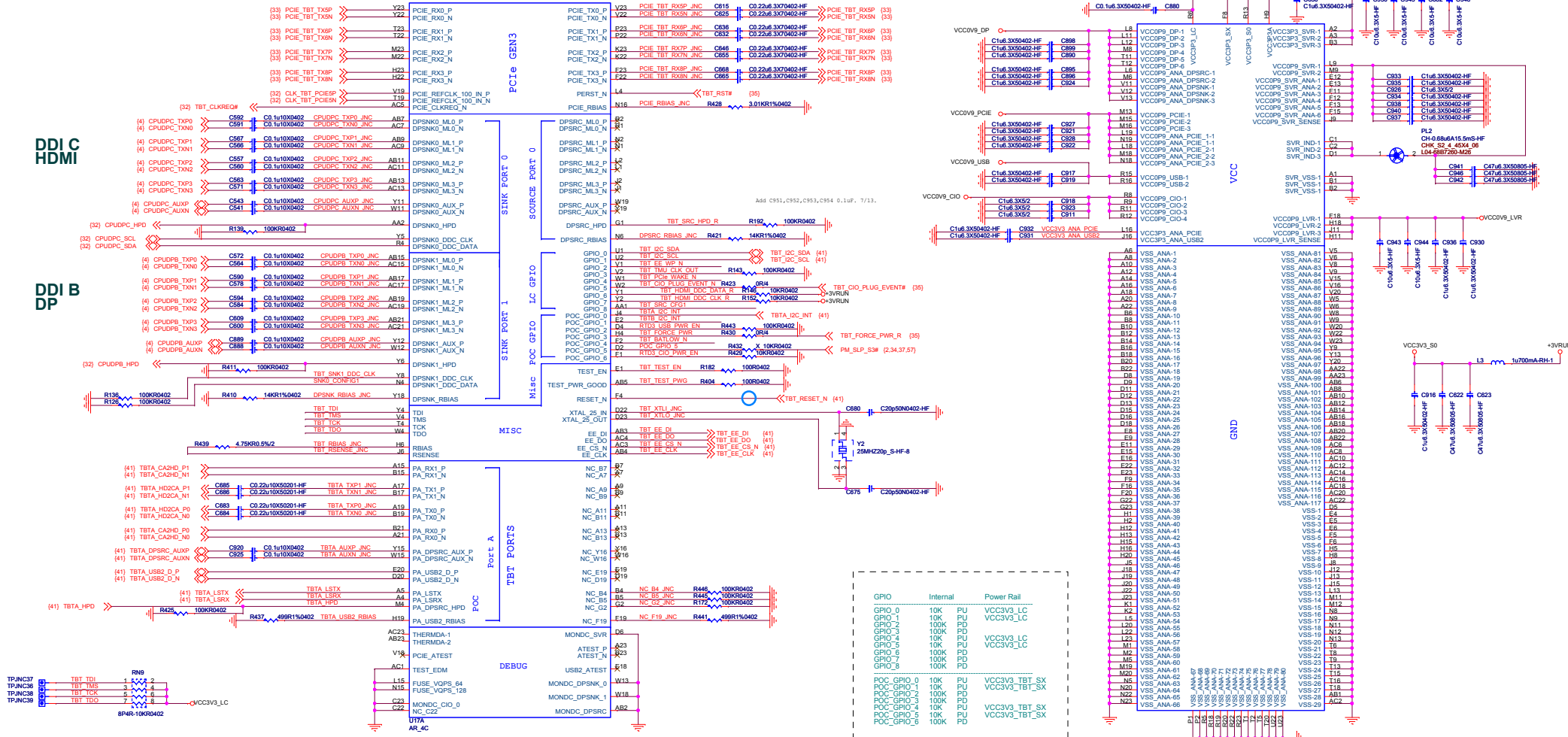
For Sharp14" QHD

SPEC:
VF=20.8~24V
If , one channel = 19.8mA

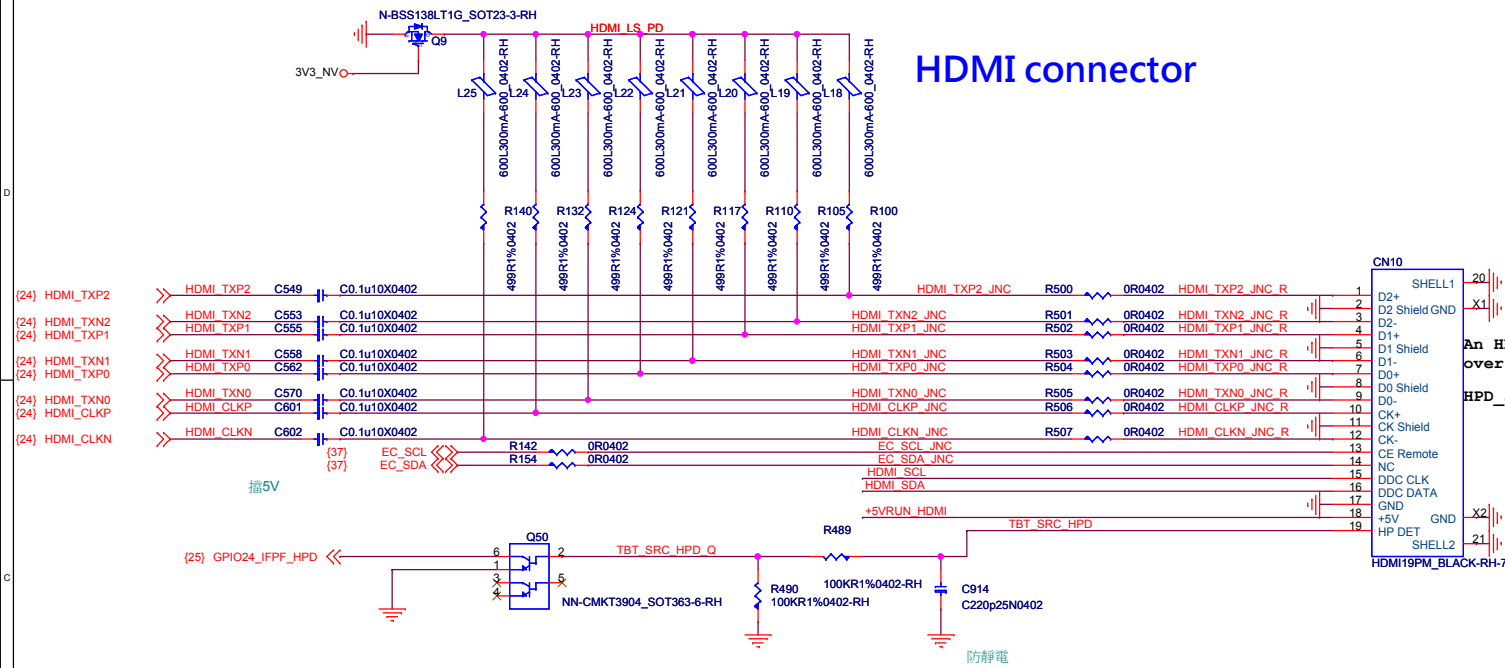


NC U43 G5968 function. 5/13.

Thunderbolt

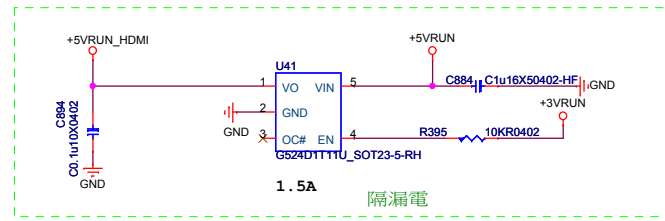
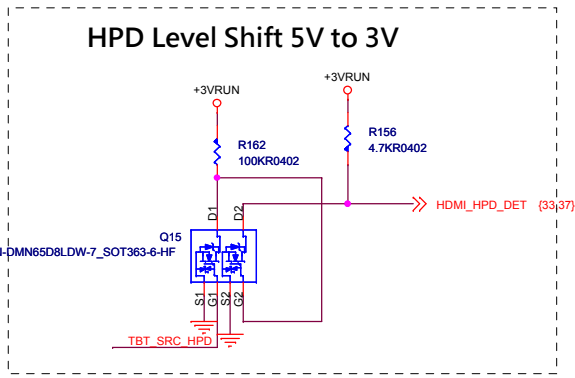
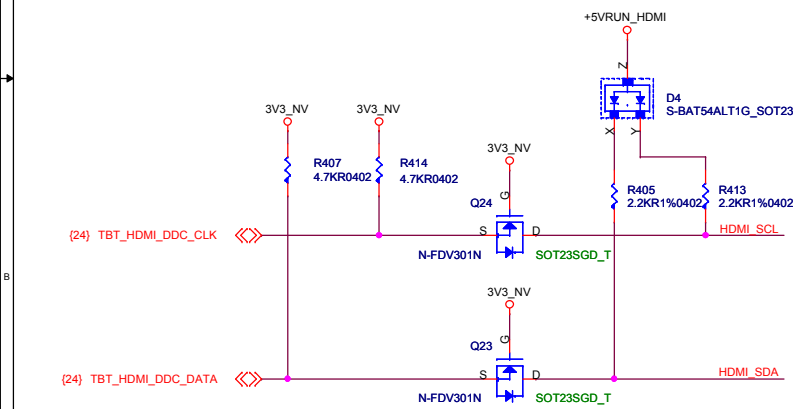


HDMI connector

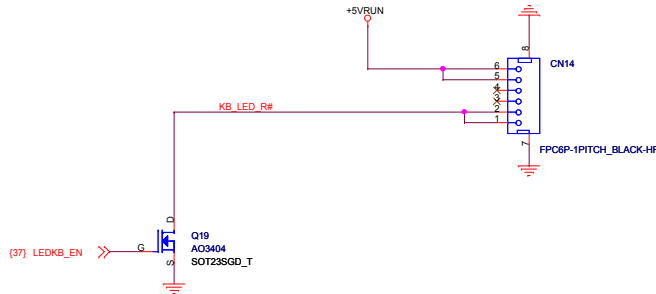


An HDMI Source shall have +5V Power signal over-current protection of no more than 0.5A.

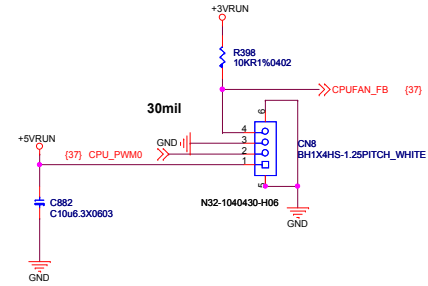
HPD_SNK Internal PD 150kohm



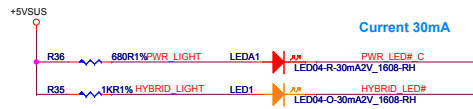
PWR SW/CPU FAN/BTB CONN/ LED CONN



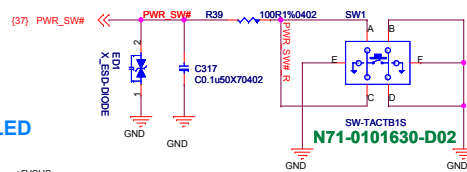
CPU FAN



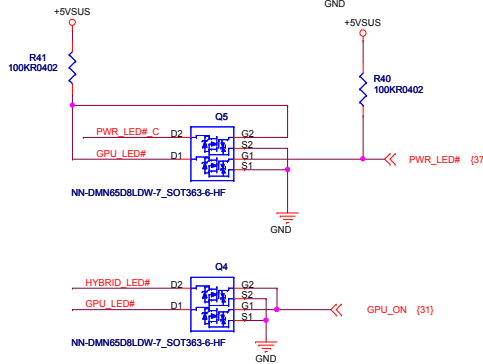
Power LED



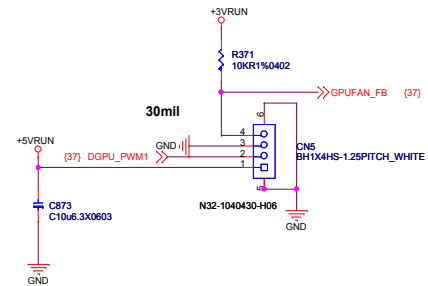
Power Switch



Control PWR LED

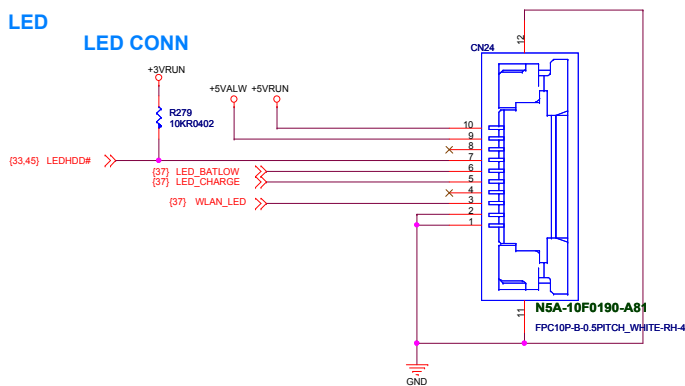


DGPU FAN

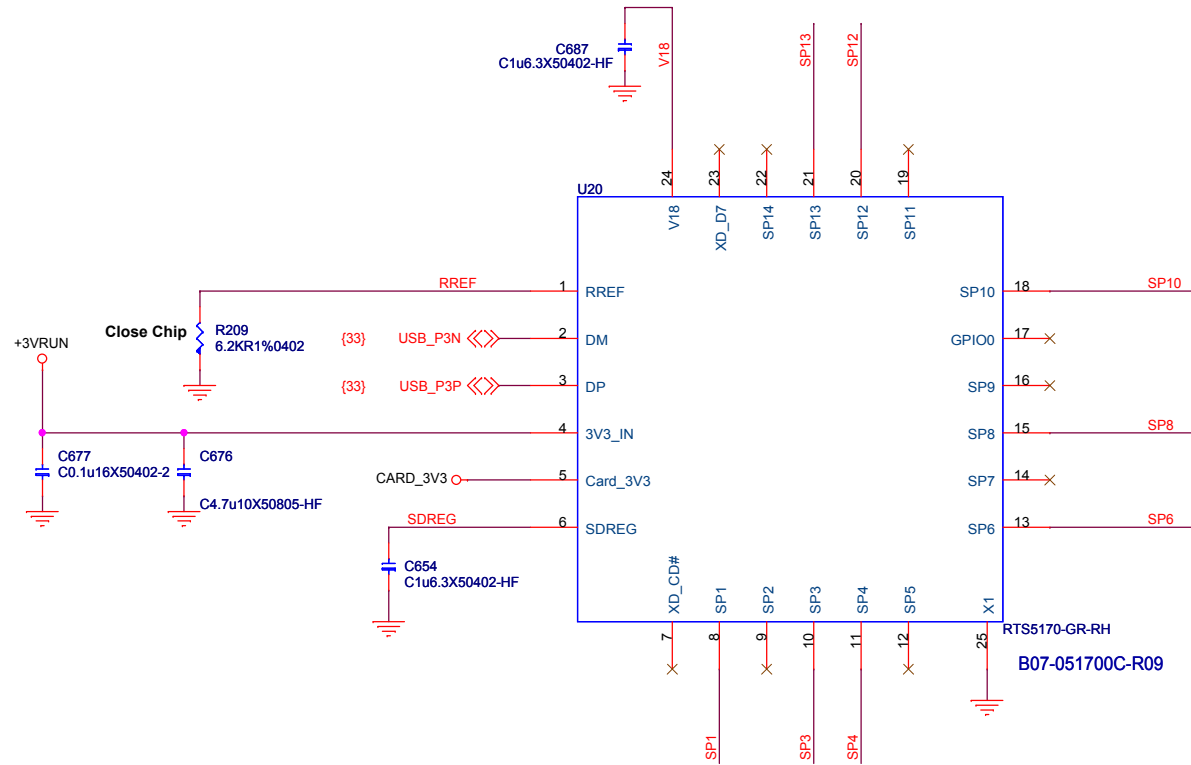


LED

LED CONN

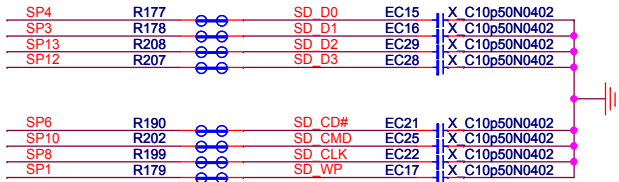


CardReader (RTS5170)

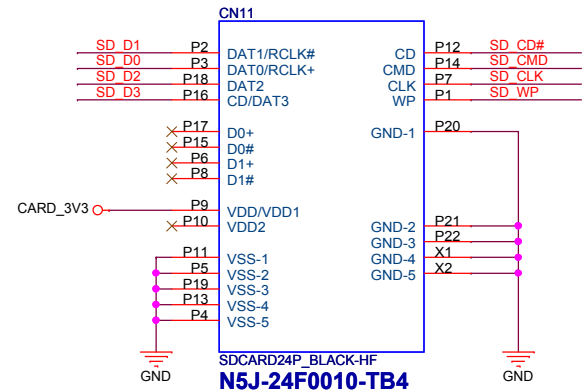
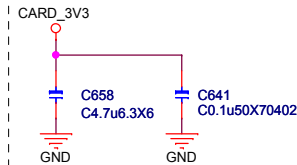


CARD_3V3: 950mA

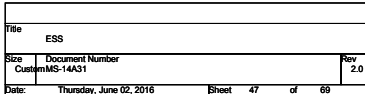
For EMI and Close to RTS5170



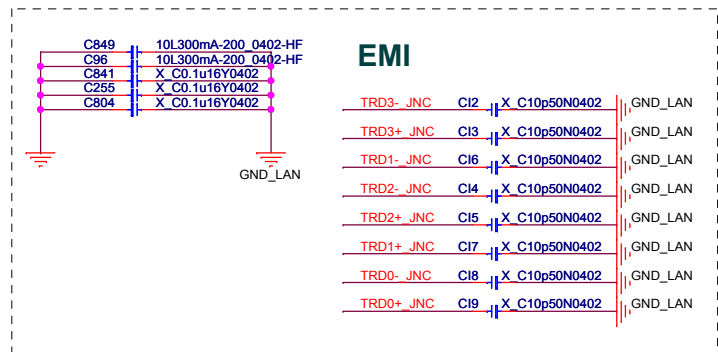
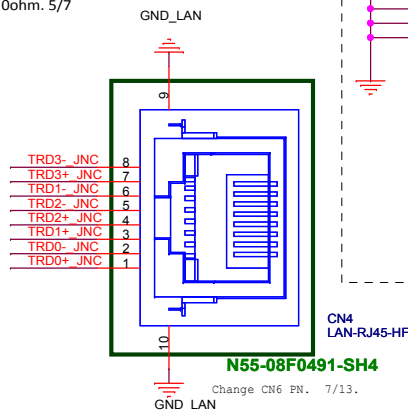
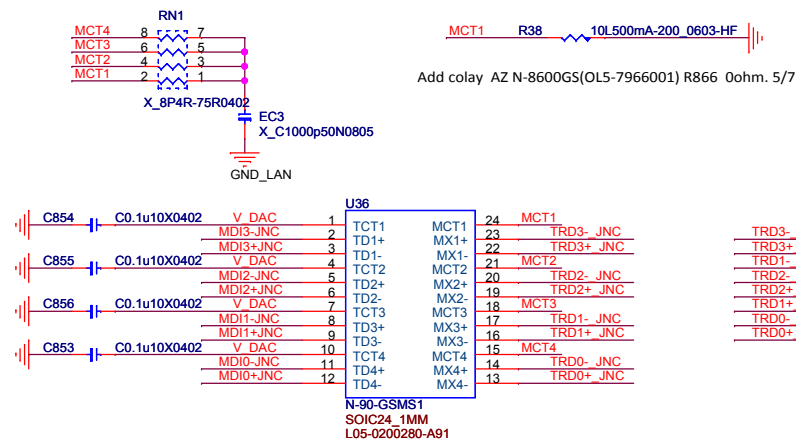
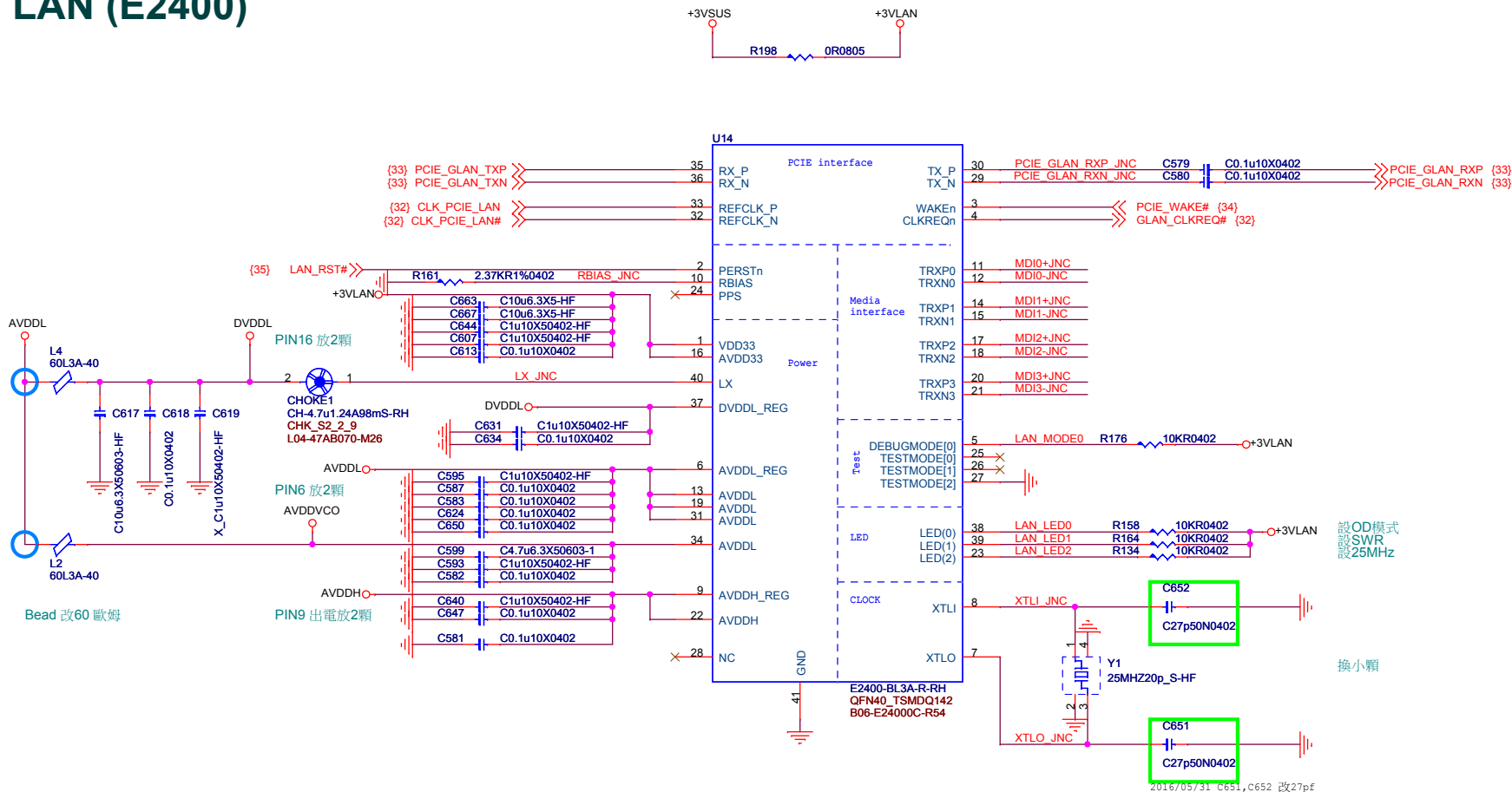
Close Connector



05/09 R264, R265, R280, R284 change to 0ohm



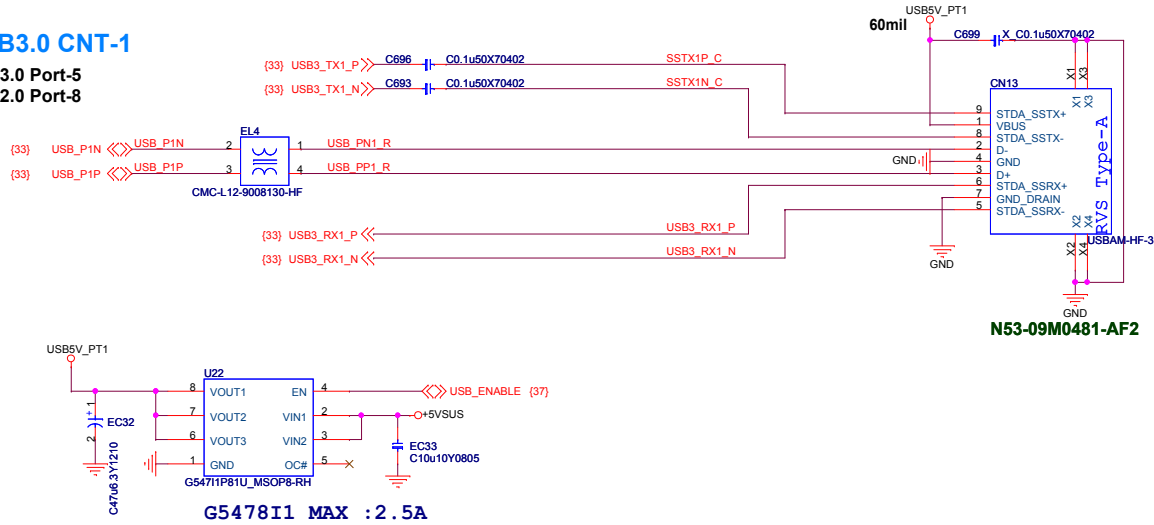
LAN (E2400)



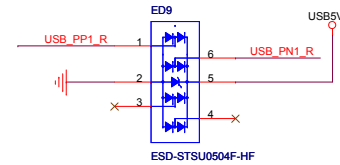
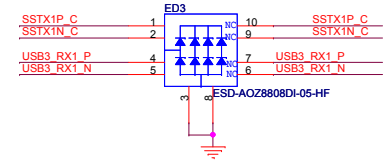
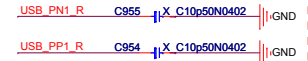
USB2.0/USB 3.0

USB3.0 CNT-1

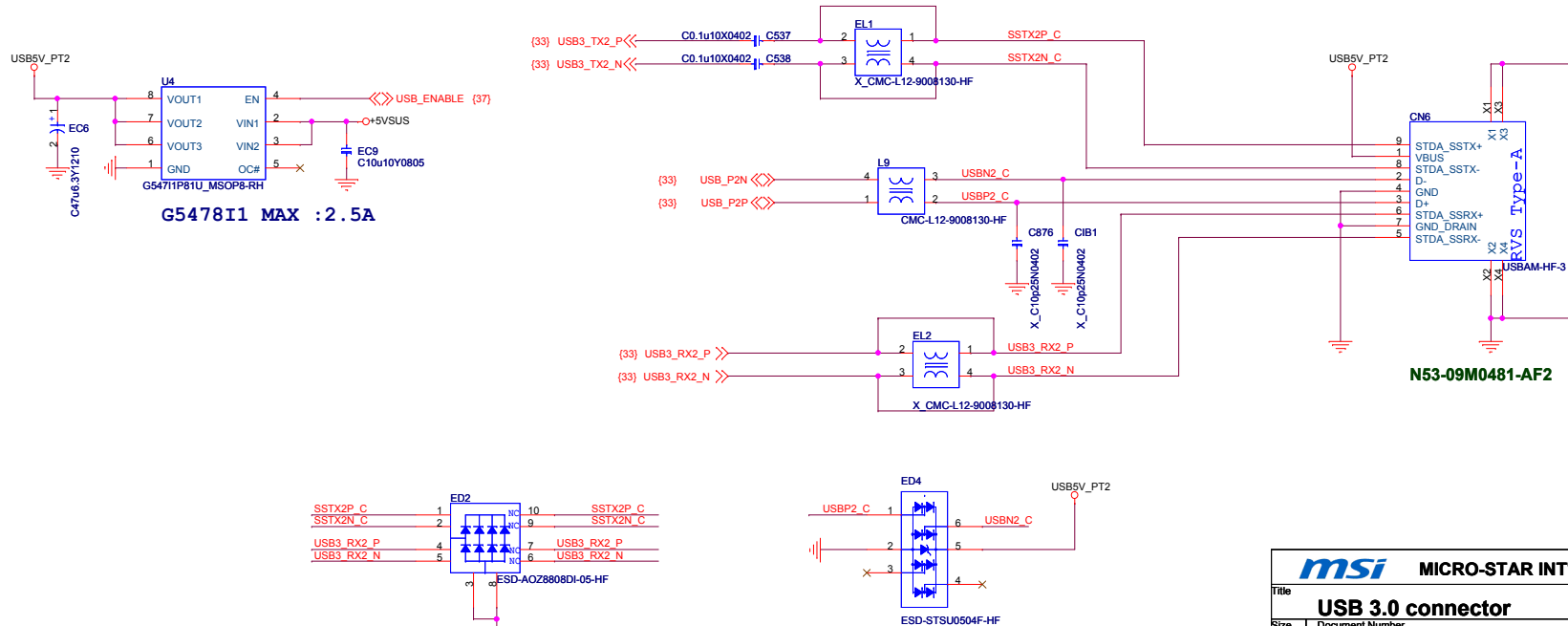
USB3.0 Port-5
USB2.0 Port-8



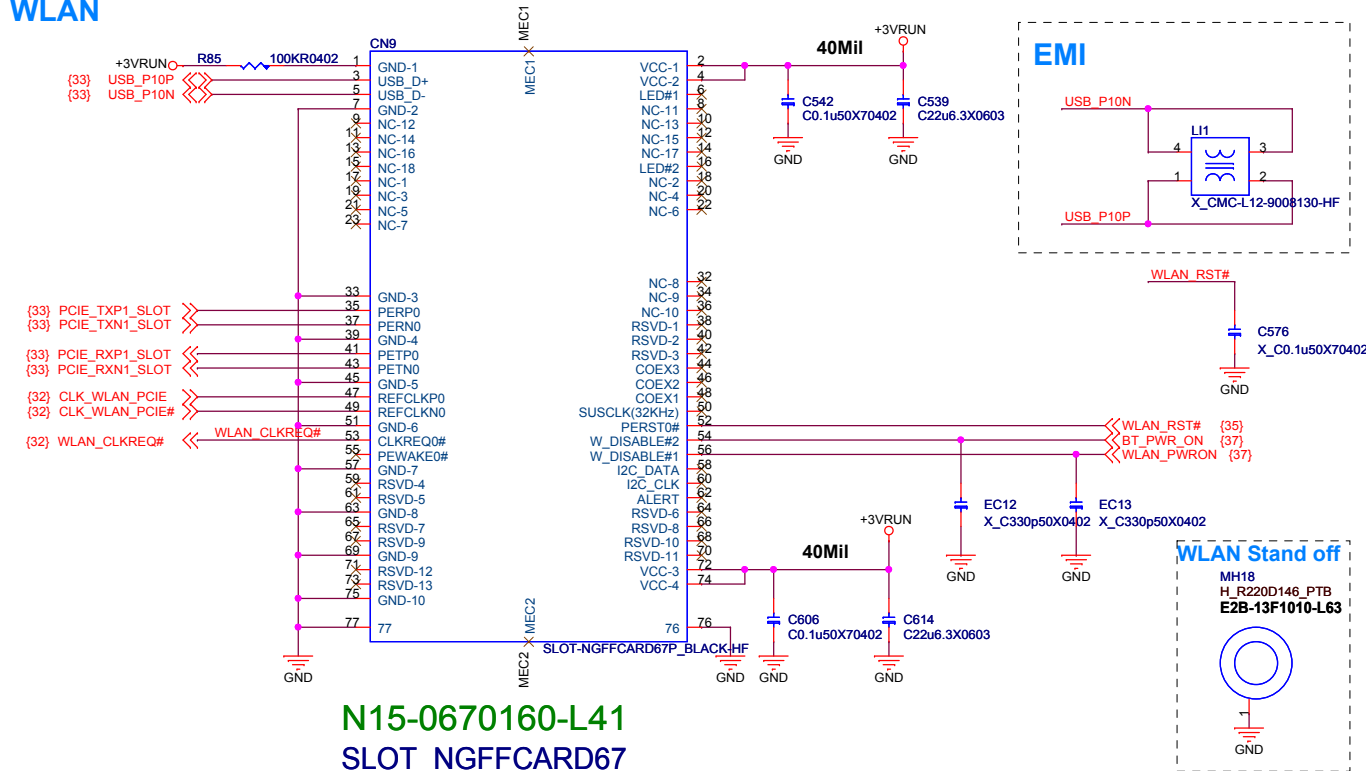
EMI



USB 3.0 CNT 2



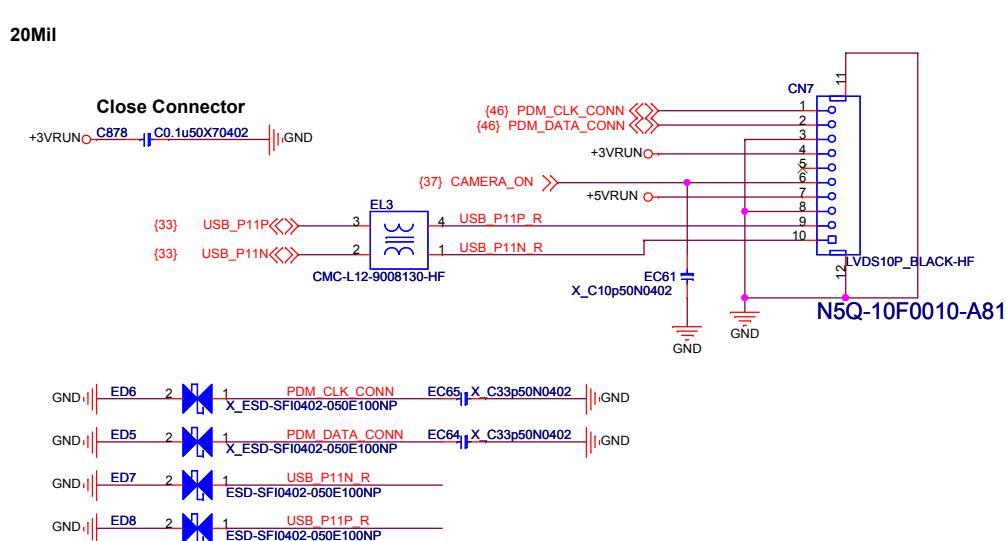
WLAN



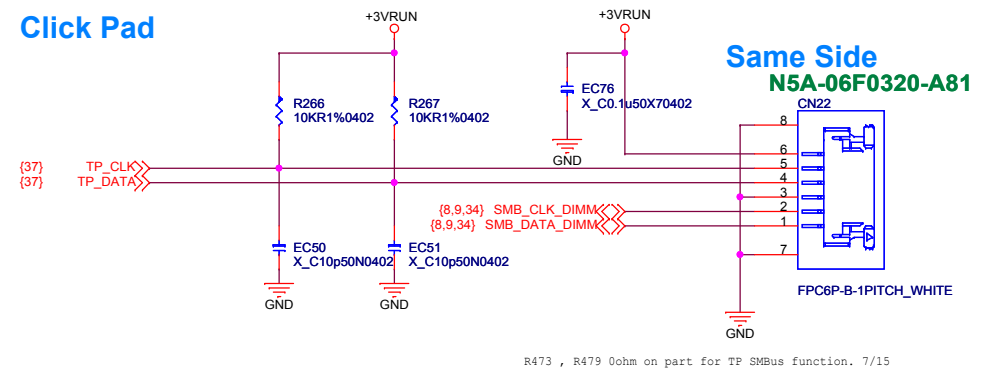
Pin 1	GND	Pin 6	LED1#
Pin 3	USB_D+	Pin 8	Module Key
Pin 5	USB_D-	Pin 10	Module Key
Pin 7	GND	Pin 12	Module Key
Pin 9	Module Key	Pin 14	Module Key
Pin 11	Module Key	Pin 16	LED2#
Pin 13	Module Key	Pin 18	GND
Pin 15	N/C	Pin 20	N/C
Pin 17	N/C	Pin 22	N/C
Pin 19	N/C	Pin 24	Module Key
Pin 21	N/C	Pin 26	Module Key
Pin 23	N/C	Pin 28	Module Key
Pin 25	Module Key	Pin 30	Module Key
Pin 27	Module Key		
Pin 29	Module Key		
Pin 31	Module Key		
Pin 33	GND	Pin 32	N/C
Pin 35	PERP0	Pin 34	N/C
Pin 37	PERN0	Pin 36	N/C
Pin 39	GND	Pin 38	Clink Reset (I 3.3V)
Pin 41	PETP0	Pin 40	N/C
Pin 43	PETN0	Pin 42	N/C
Pin 45	GND	Pin 44	N/C
Pin 47	REFCLKP0	Pin 46	N/C
Pin 49	REFCLKN0	Pin 48	N/C
Pin 51	GND	Pin 50	N/C (SUSCLK (32kHz) for DSx)
Pin 53	CLKREQ0#	Pin 52	PERST0#
Pin 55	PEWAKE0#	Pin 54	BT_EN (W_DISABLE2#)
Pin 57	GND	Pin 56	WLAN_EN (W_DISABLE2#)
Pin 59	N/C	Pin 58	N/C
Pin 61	N/C	Pin 60	N/C
Pin 63	GND	Pin 62	N/C
Pin 65	N/C	Pin 64	Resever
Pin 67	N/C	Pin 66	N/C
Pin 69	GND	Pin 68	N/C
Pin 71	N/C	Pin 70	N/C
Pin 73	N/C	Pin 72	3.3V
Pin 75	GND	Pin 74	3.3V

CAMERA

20Mil

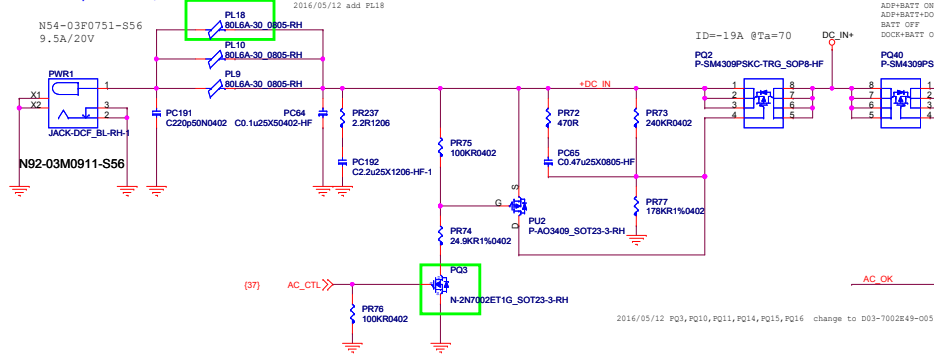


Click Pad

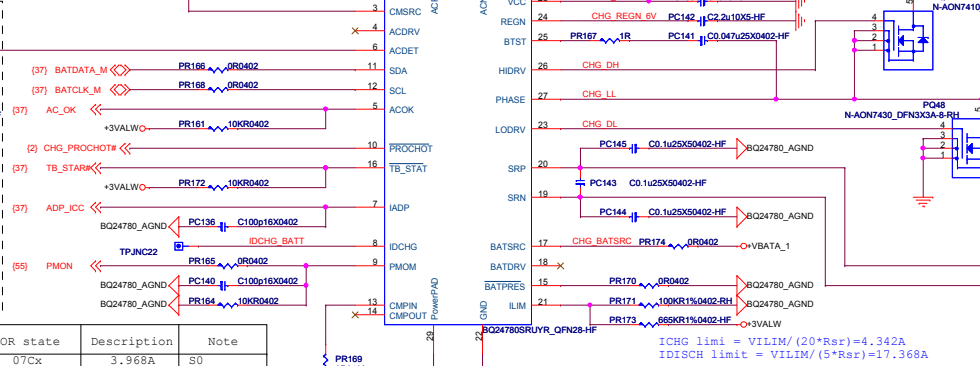
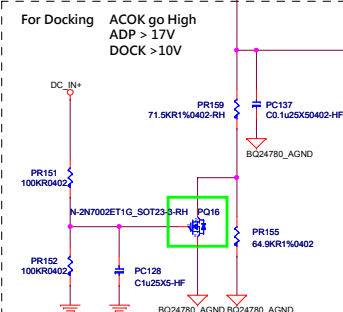
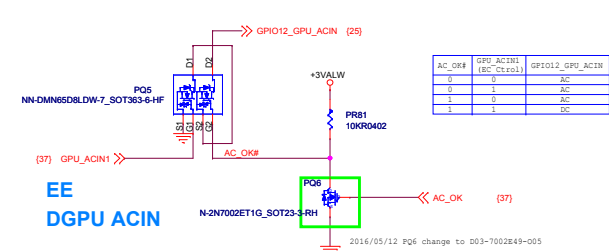
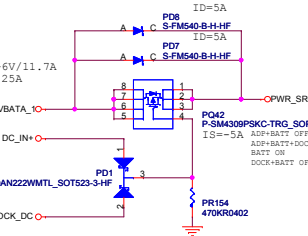
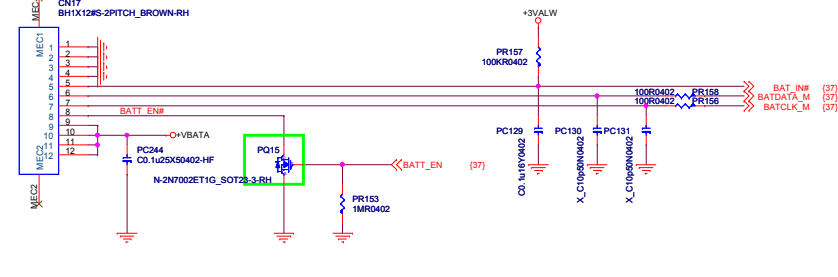


R473 , R479 0ohm on part for TP SMBus function. 7/15

180W, 19.5V/9.23A

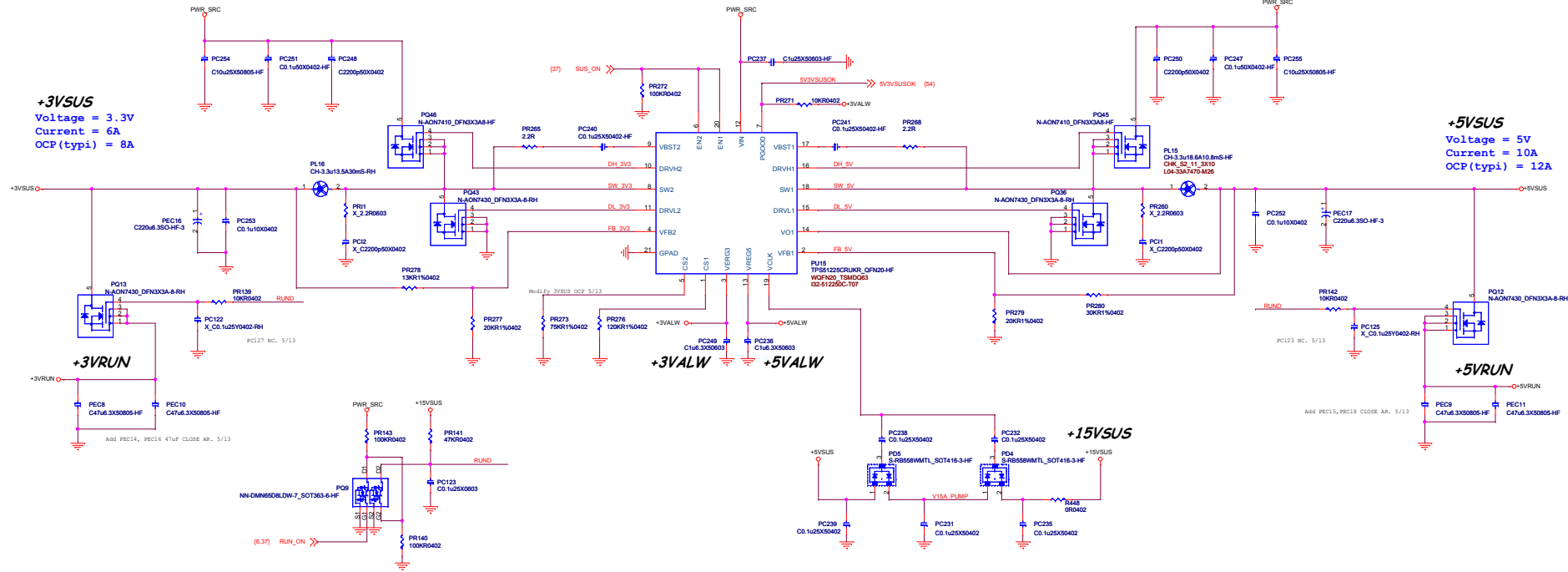


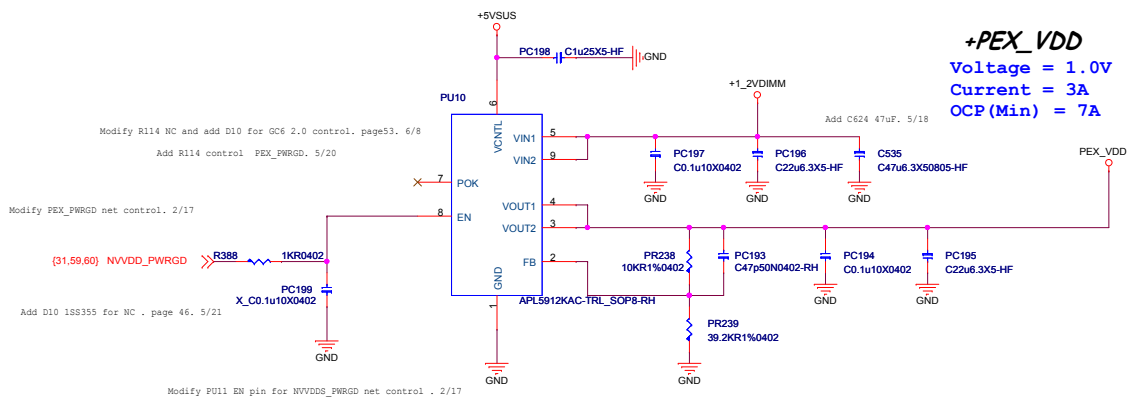
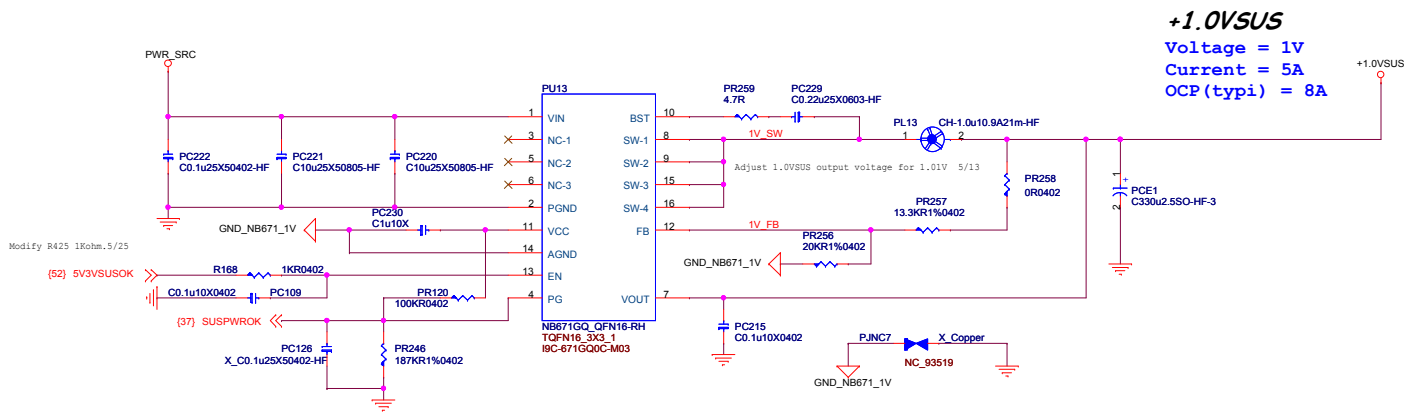
2S2P, 70W/6V=11.66A



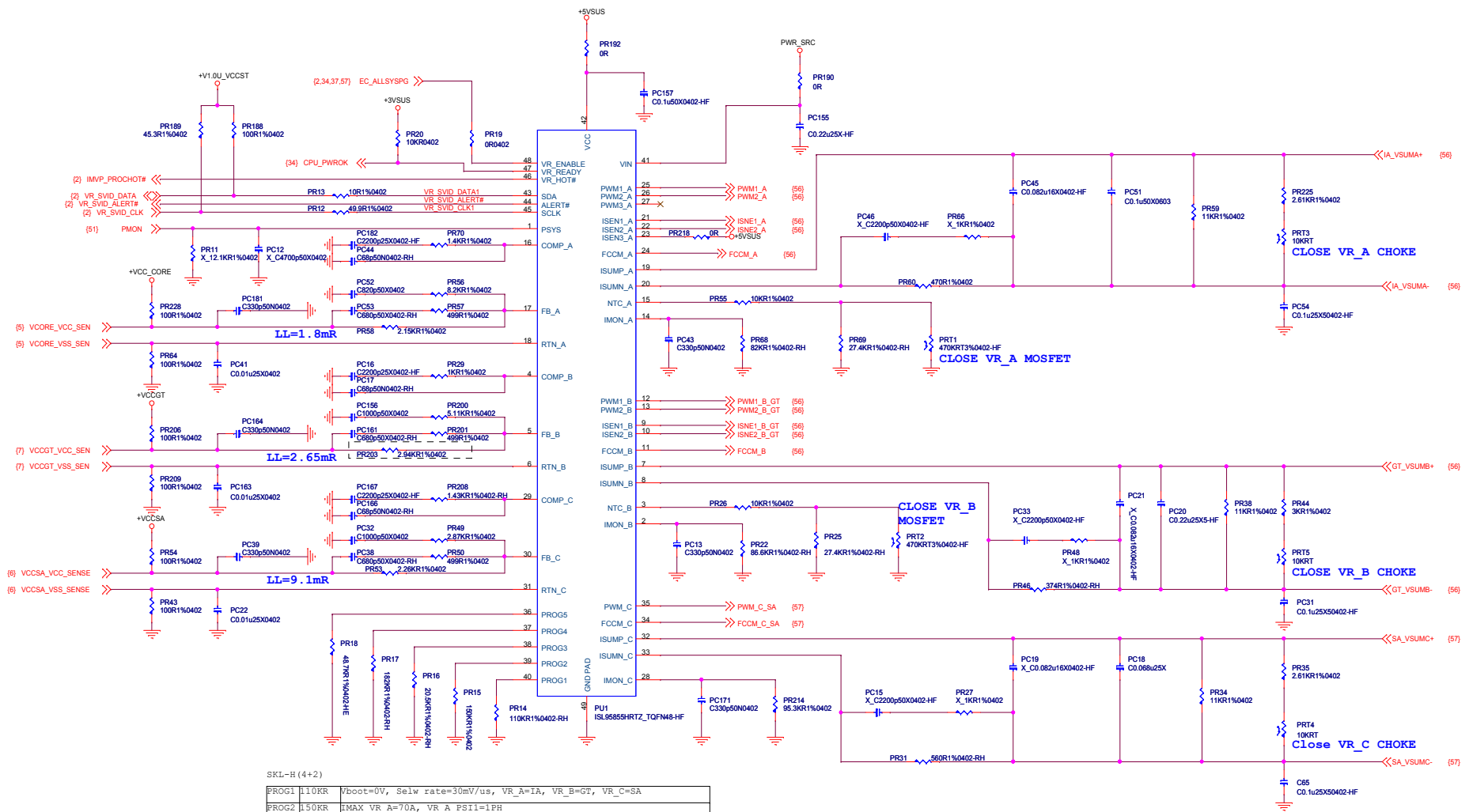
Register name	Register address	POR state	Description	Note
Charge current (5mR)	0x14H	07Cx	3.968A	S0
Prepare charge (5mR)	0x14H	004x	0.128A	S3/S4/S5
Input current (5mR)	0x3FH	19.5V 120x	9.216A	180W
		12V 098x	4.864A	65W
Charge voltage	0x15H	220x	8.7V	2S2P
Discharge current (5mR)	0x39H	008x	2.048A	BOOST current

Voltage = 8.7V for 2S2P
Charge Current = 4.03A
Discharge Current = 11.66A

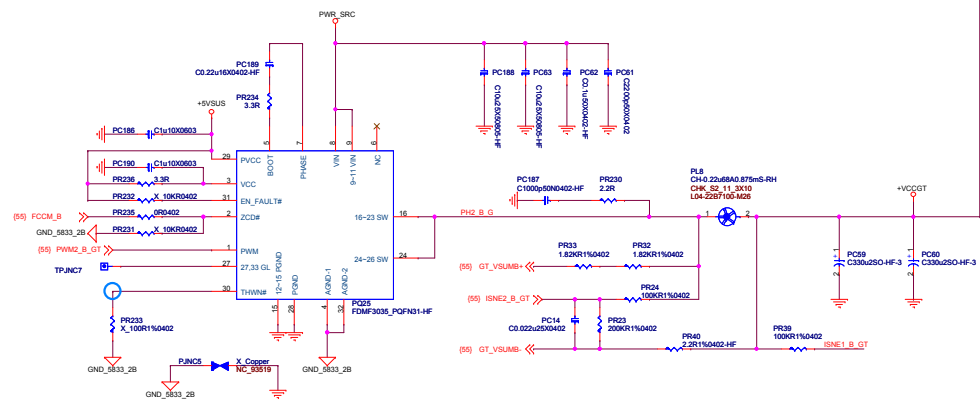
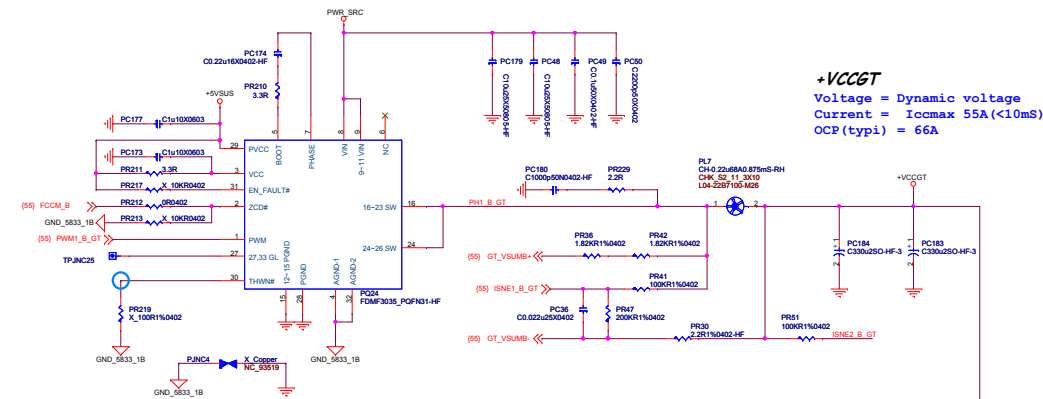
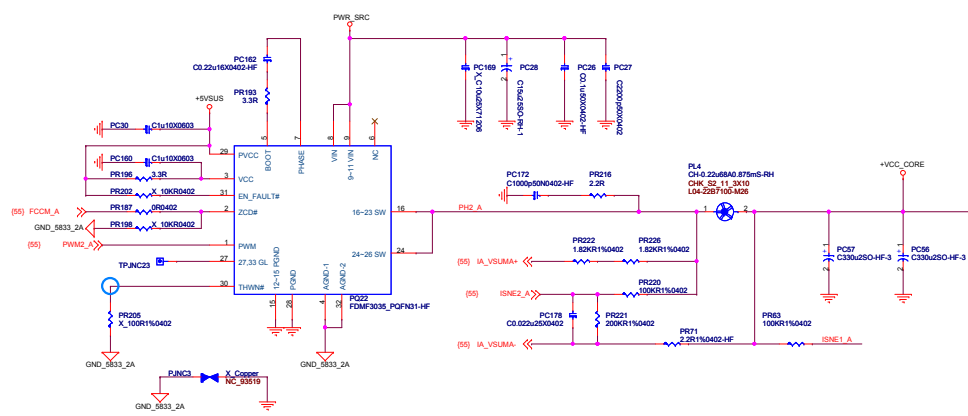
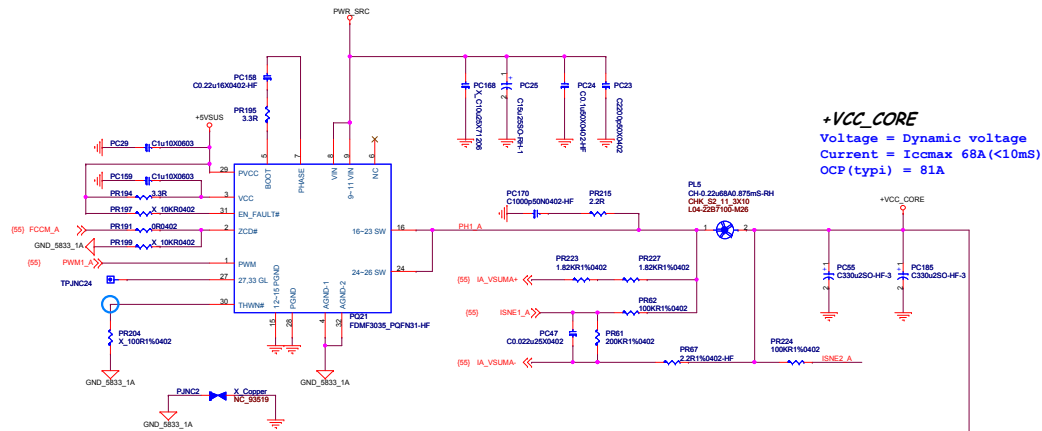


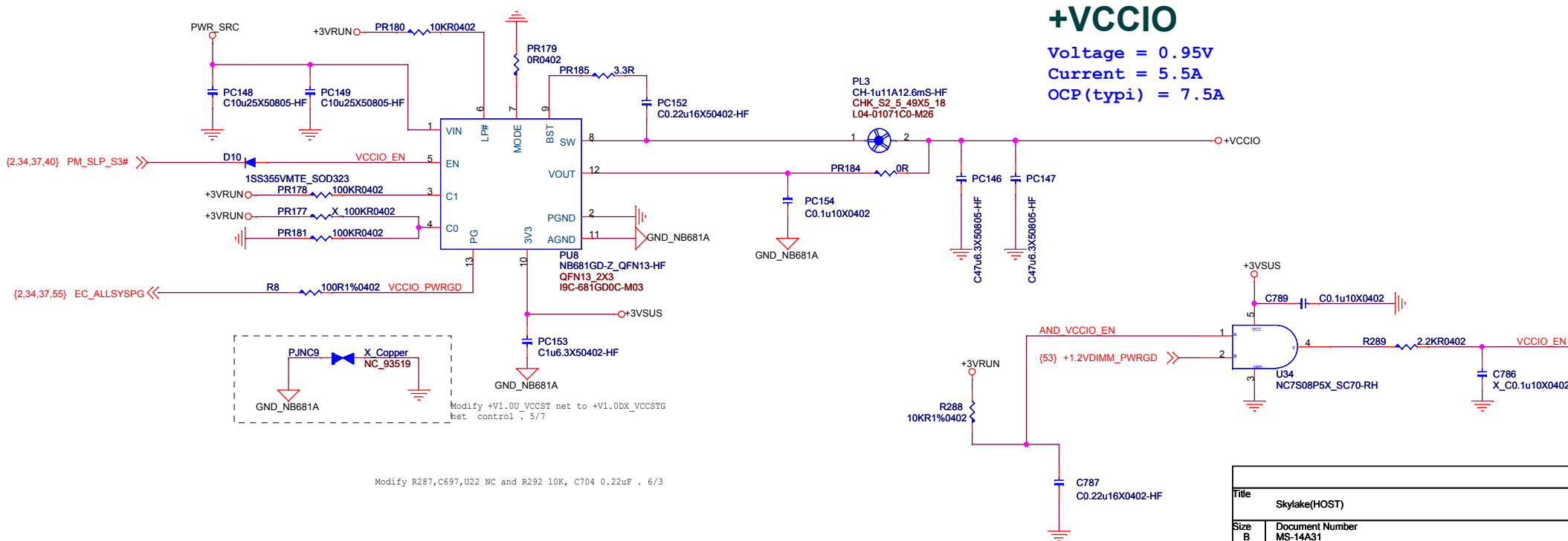
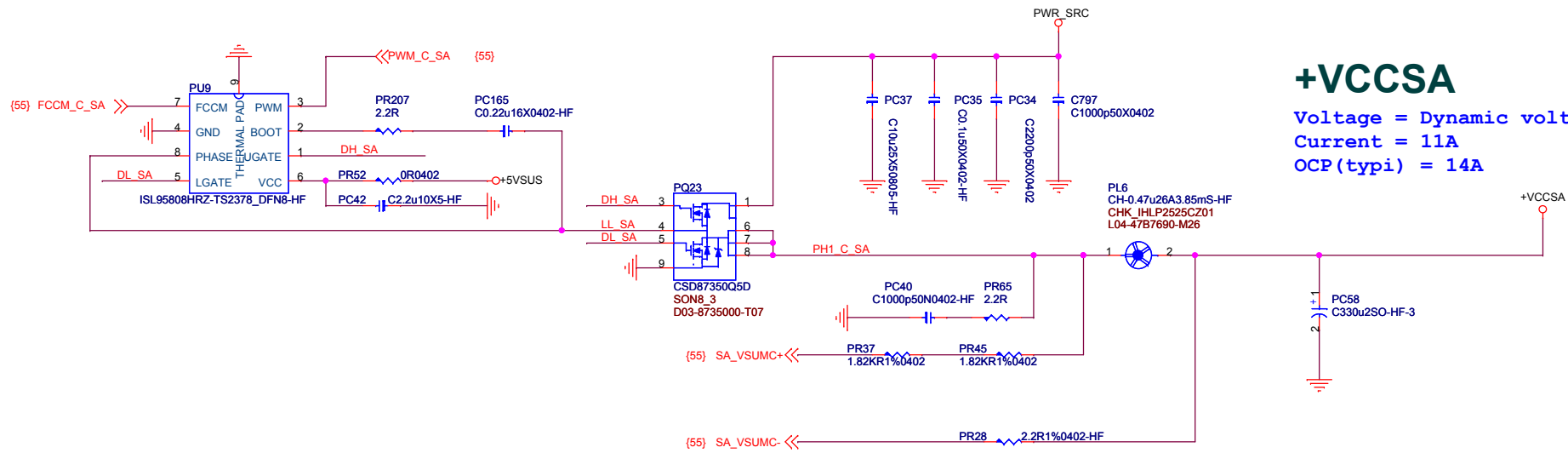


Skylake H-line 42 45W ISL95855

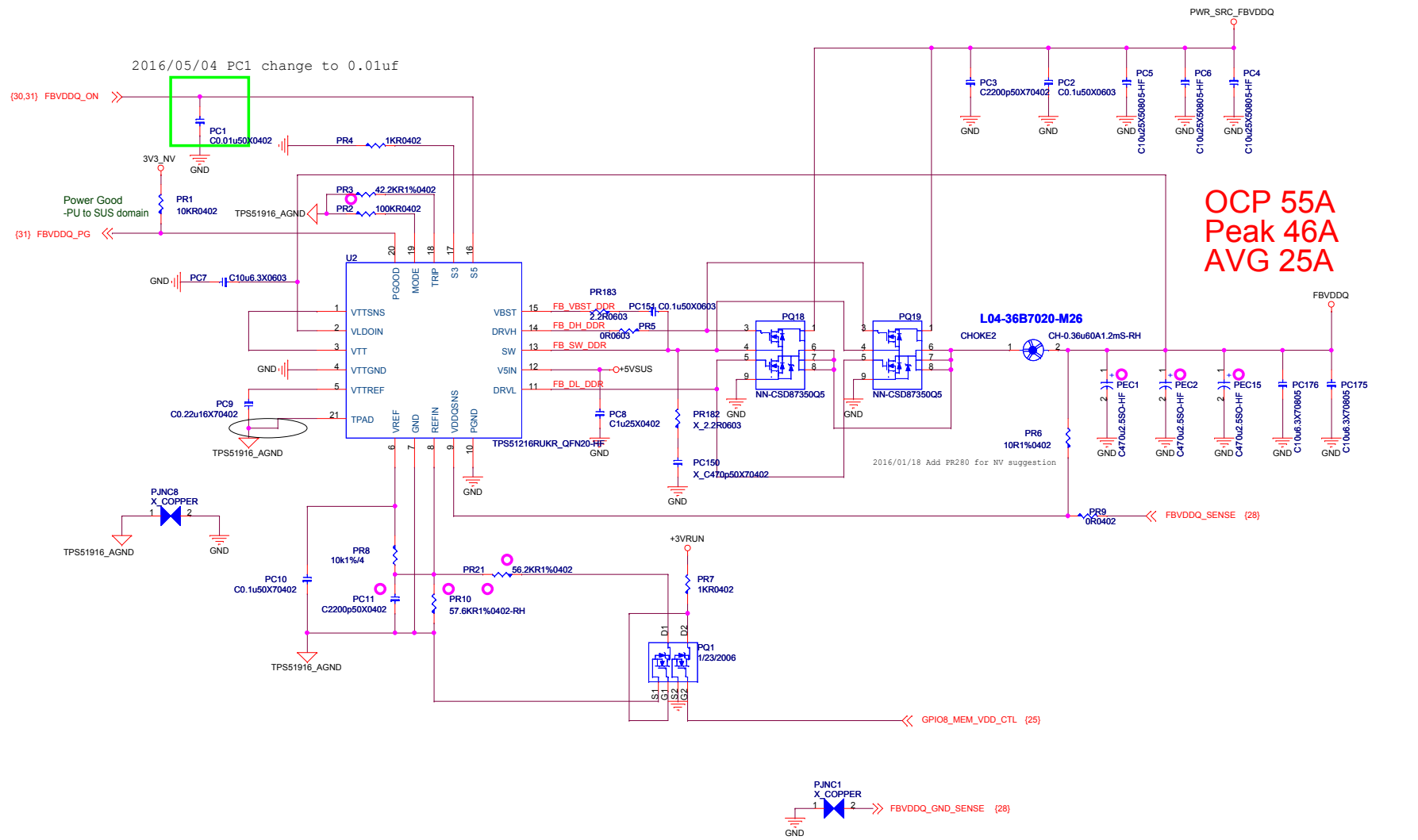


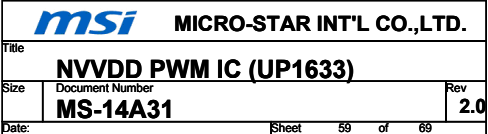
```
SKL-H (4+2)
PROG1 110KR Vboot=0V, Selw rate=30mV/us, VR_A=IA, VR_B=CT, VR_C=SA
PROG2 150KR IMAX VR_C=70A, VR_A PS1=1PH
PROG3 20.5KR IMAX VR_B=60A, DROOP VR_B Active
PROG4 182KR DROOP VR_A Active, DROOP VR_C Active, VR_A VR_B Frequency=750KHz
PROG5 48.7KR IMAX VR_C=12A, Frequency=450KHz
```

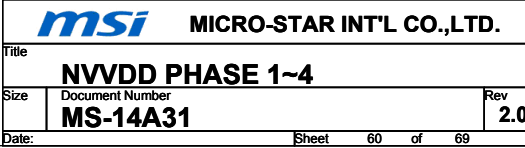


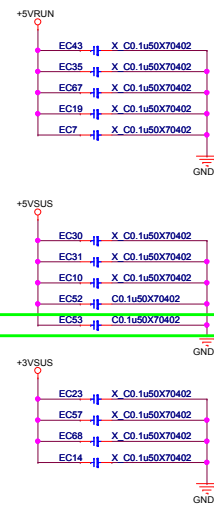
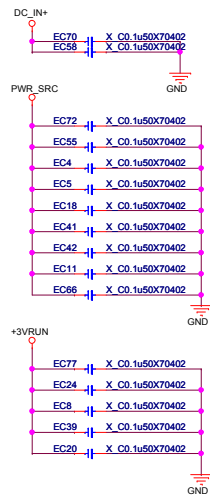


Title		
Skylake(HOST)		
Size	Document Number	Rev
B	MS-14A31	2.0
Date:	Thursday, June 02, 2016	Sheet 57 of 69

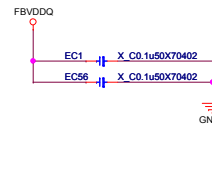








Add EC74 0.1uF for EMI.5/22



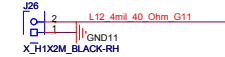
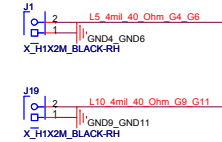
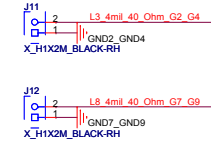
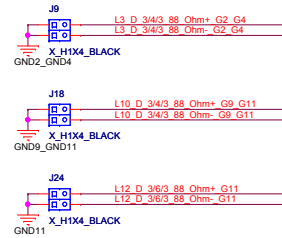
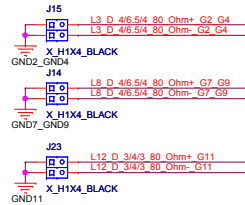
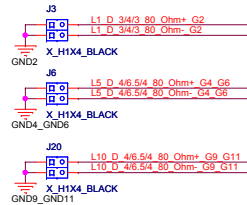
E4	E5
E2Y-X022911-CA7	E2Y-X022911-CA7
X_GASKET	X_GASKET
E6	E7
E2Y-X022911-CA7	E2Y-X022911-CA7
X_GASKET	X_GASKET
E9	E8
E2Y-X022911-CA7	E2Y-X022911-CA7
X_GASKET	X_GASKET

Add E4, E5, E6, E7, E8, E9 for EMI.5/22

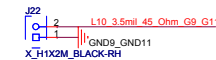
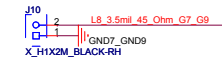
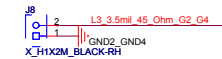
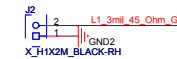
80 OHM / CLK/WCK

88 OHM /Alpine Ridge/DDR4 CLK

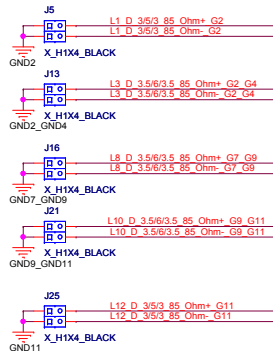
40 OHM / DDR4 CTRL



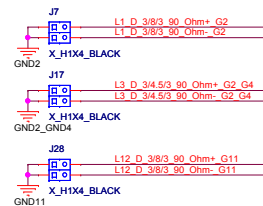
45 OHM / DDR4 Data



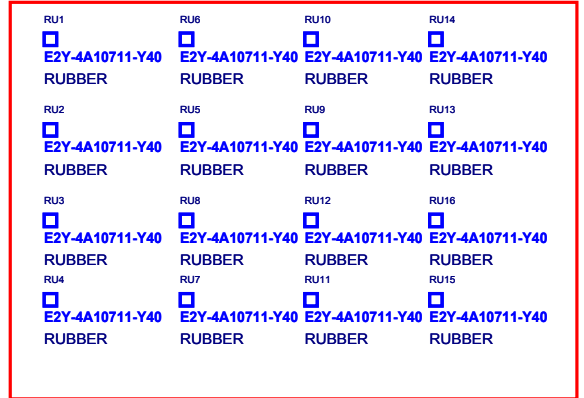
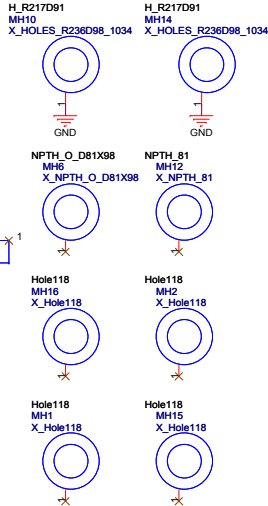
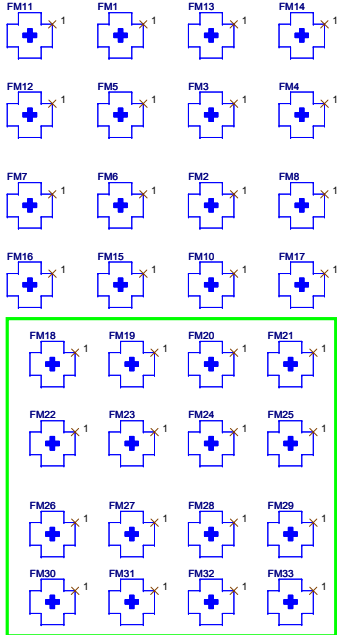
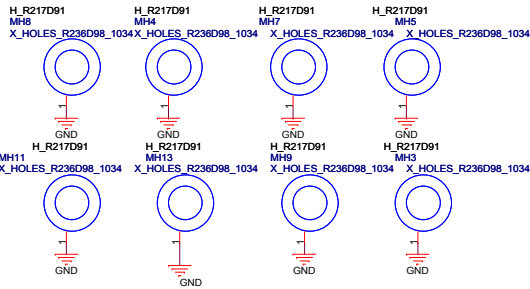
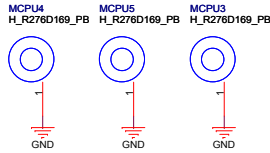
85 OHM /SATA /PCH PCIE/ EDP USB /HDMI/DP/DMI/CLK/PEG



9 AR type-C



CPU Holes



E2M-4A11411-A89



E2M-4A11311-A89



E2Y-X050411-G40



E2P-4A11411-Y42



E2Y-4A11011-Y42



X_E2P-4A10711-G40E2P-0112911-Y42



E2P-0112911-Y42

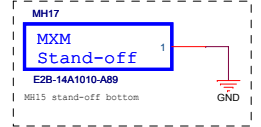
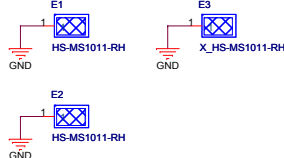
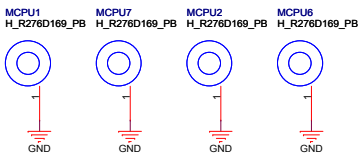


E2P-0112911-Y42



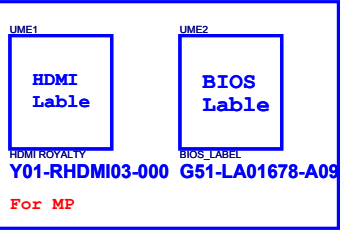
E2Y-4A11011-Y42

DGPU Holes



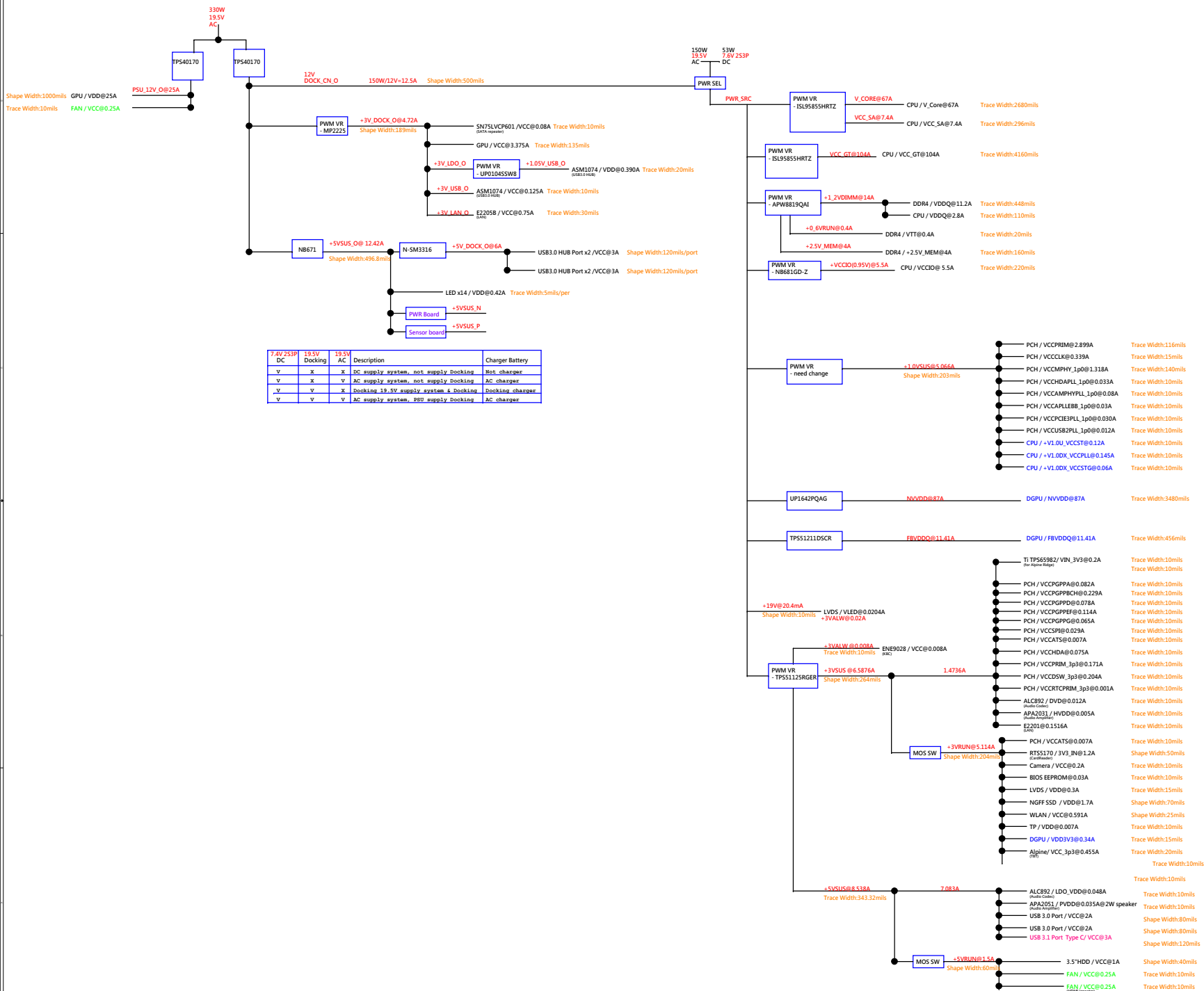
PD0-14A3120-H73

Hannstar:PD0-14A3120-H73
TRIPOD: PD0-14A3120-T53



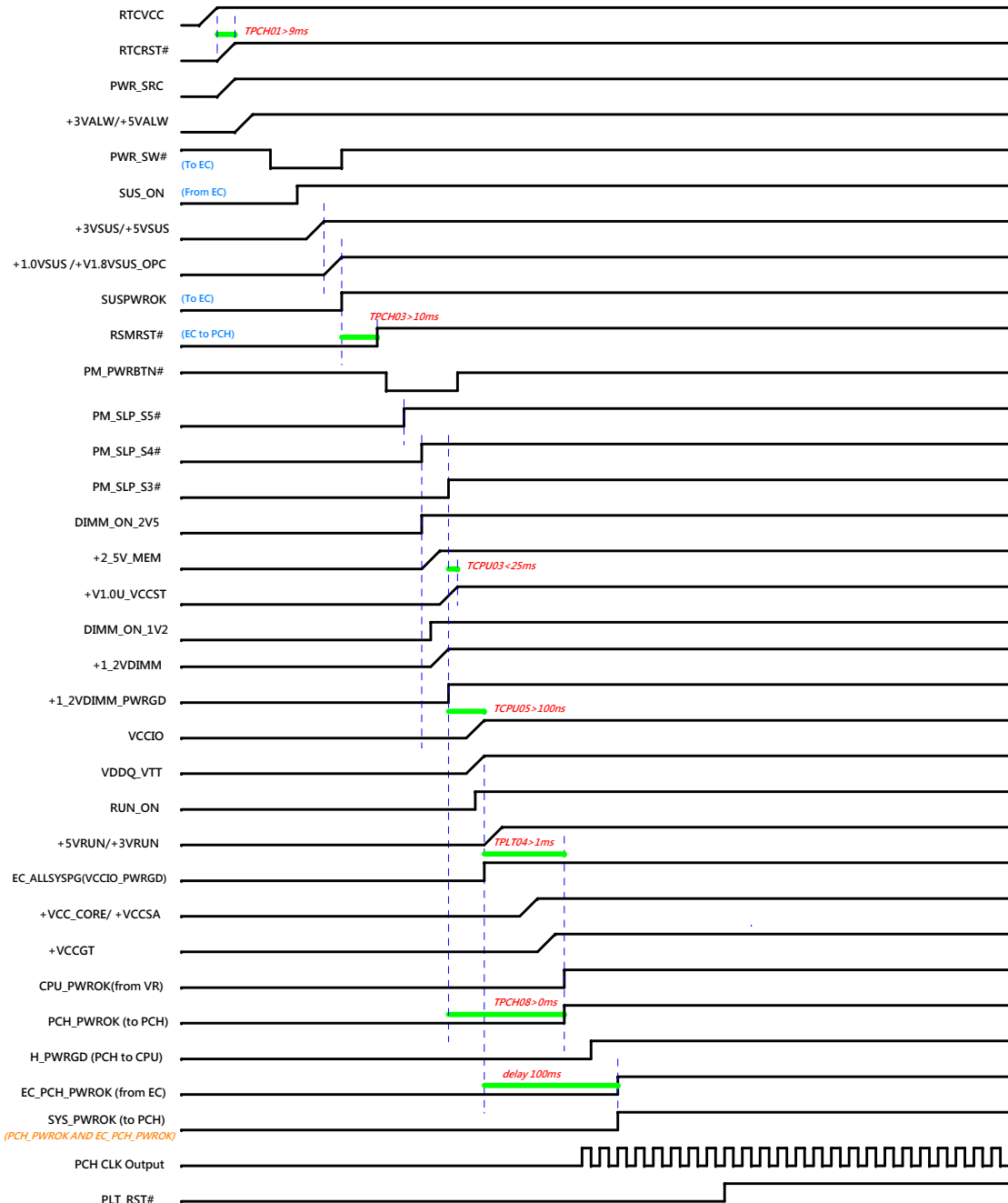
Y01-RHDMI03-000 G51-LA01678-A09
For MP

MS-14A3 Power Delivery Chart

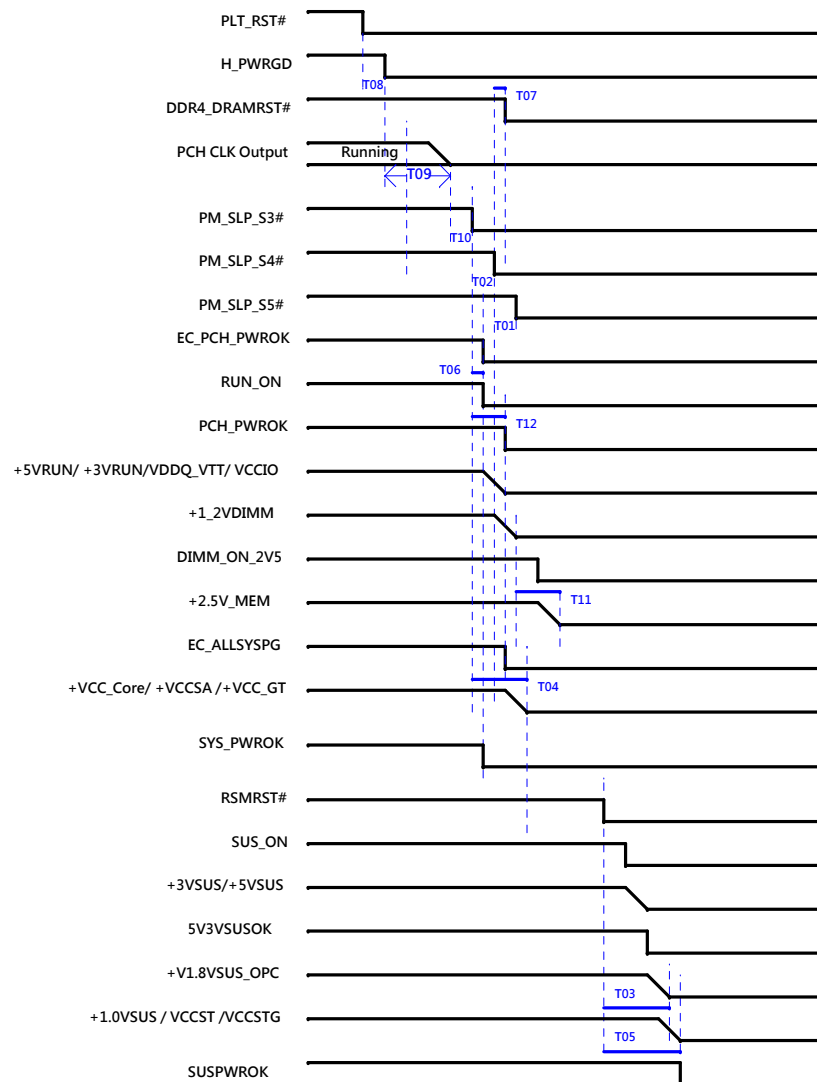


Power on Sequence

G3 -> S0

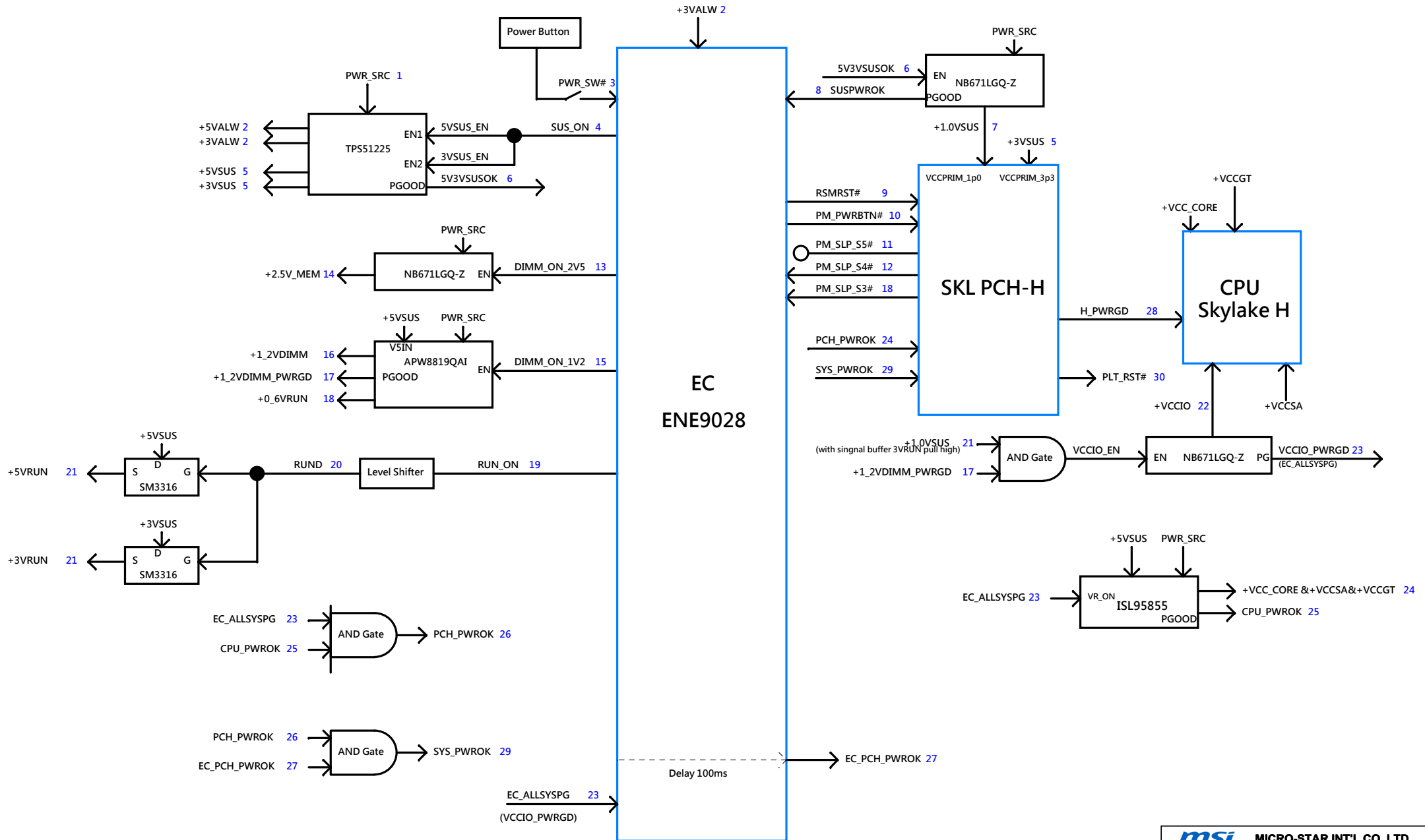


S0 -> G3



	MIN	MAX	Units	Description
T01	30		us	SLP_S5# assertion to SLP_S4#
T02	30		us	SLP_S4# assertion to SLP_S3#
T03	1		us	RSMRST# asserting to VccPRIM dropping 5% of nominal value
T04		500	ms	SLP_S3# assertion to VCC, VCCGT, VCCIO and VCCSA rails completely off.
T05	1		us	RSMRST# asserting to VccPRIM dropping 5% of nominal value
T06		1	us	SLP_S3# assertion to VCCIO VR disabled
T07	-100		ns	DDR_RESET# assertion to SLP_S4# assertion
T08	30		us	PLTRST# assertion to PROCPWRGD deassertion
T09	10		us	PROCPWRGD de-assertion to CLKOUT_BCLK turning OFF.
T10	1		us	CLKOUT_BCLK turning OFF to SLP_S3# assertion
T11	30		ms	VDDQ ramped down to VPP ramp down
T12	0		ms	SLP_S3# assertion to PCH_PWROK deassertion

MS-14A3 Power on Block Diagram



History

08:

2016/05/04

1.Add D12・D13・D14・R485・R486・C1003
2.PR244 Change 10kohm,R191・R75 Change 47Kohm,PC1・C529 Change 0.01uf,R74 Change 0ohm
3.Y3 Change to D05-2801600-T02
4.C525 NC

2016/05/06

1.Add PR284・PR285

2016/05/09

1.R264, R265, R280, R284 change to 0ohm

2016/05/17

1.PR108 change to 620ohm,PR113 change to 1Kohm,PR121 change to 3.3Kohm